SAM2634

LOW-POWER SYNTHESIZER WITH EFFECTS

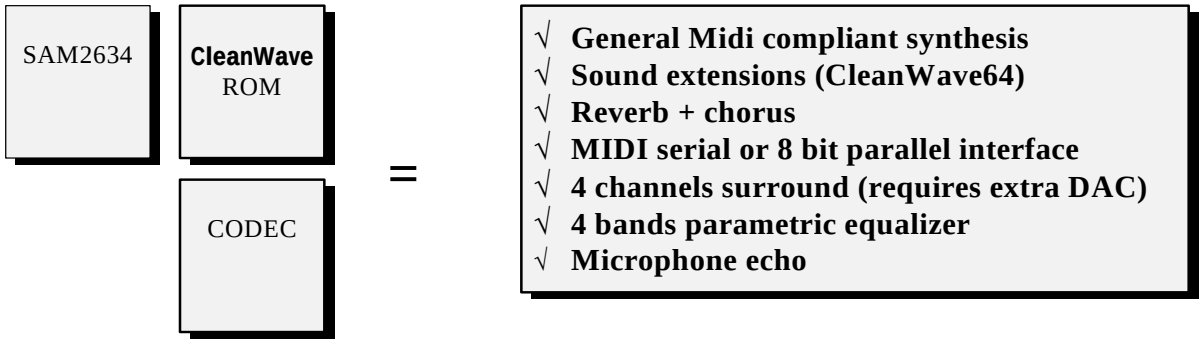
The SAM2634 integrates into a single chip a proprietary **DREAM®** DSP core (64-slots DSP + 16-bit microcontroller), a 32k x 16 RAM and an LCD display interface. With addition of a single external ROM or FLASH, a complete low cost sound module can be built, including reverb and chorus effects, parametric equalizer, surround effects, without compromising on sound quality.

Key features

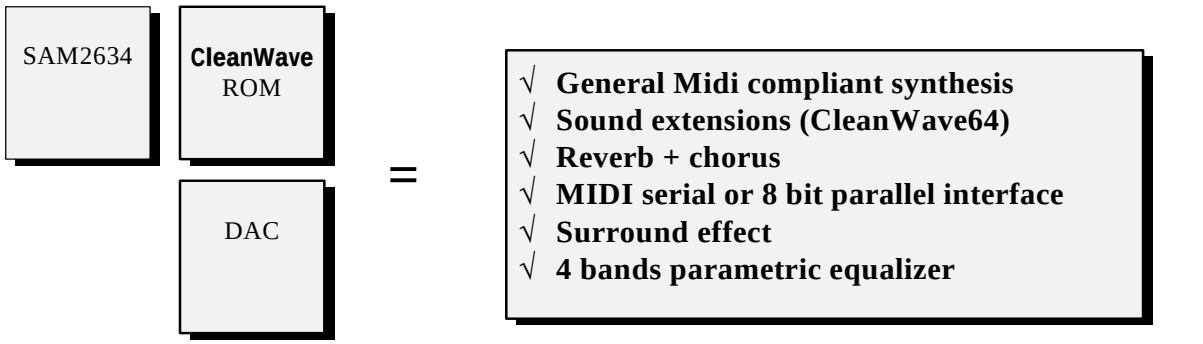
- Single chip synthesizer + effects, typical application includes:
  - Wavetable synthesis, serial MIDI in & out, parallel MIDI
  - Effects: reverb + chorus, on MIDI and/or audio in
  - Surround on 2 or 4 speakers with intensity/delay control
  - Equalizer: 4 bands, parametric
  - Audio in processing through echo, equalizer, surround
- Low chip count
  - Synthesizer, ROM/Flash, DAC
  - Effects RAM is built-in (32k x 16)
- Low power
  - 14 mA typ. operating
  - Single 3.3V supply
  - Built-in 1.2V regulator with power down mode
- High quality wavetable synthesis
  - 16 bits samples, 48 KHz sampling rate, 24dB digital filter per voice
  - Up to 64 voices polyphony
  - Up to 64MByte ROM/Flash and RAM for firmware, and PCM data
- Available wavetable firmwares and sample sets
  - CleanWave8® low cost General MIDI 1 megabyte firmware + sample set
  - CleanWave32® high quality 4 megabyte firmware + sample set
  - CleanWave64® top quality 8 megabyte firmware + sample set
  - Other sample sets available under special conditions.
- Fast product to market
  - Enhanced P16 processor with C compiler
  - Built-in ROM debugger
  - Flash programmer through dedicated pins.
- Small footprint
  - 100-pin LQFP package
- Typical applications
  - Computer karaokes, portable karaokes
  - Keyboards, portable keyboards instruments
  - Digital Drums

1- TYPICAL DESIGN

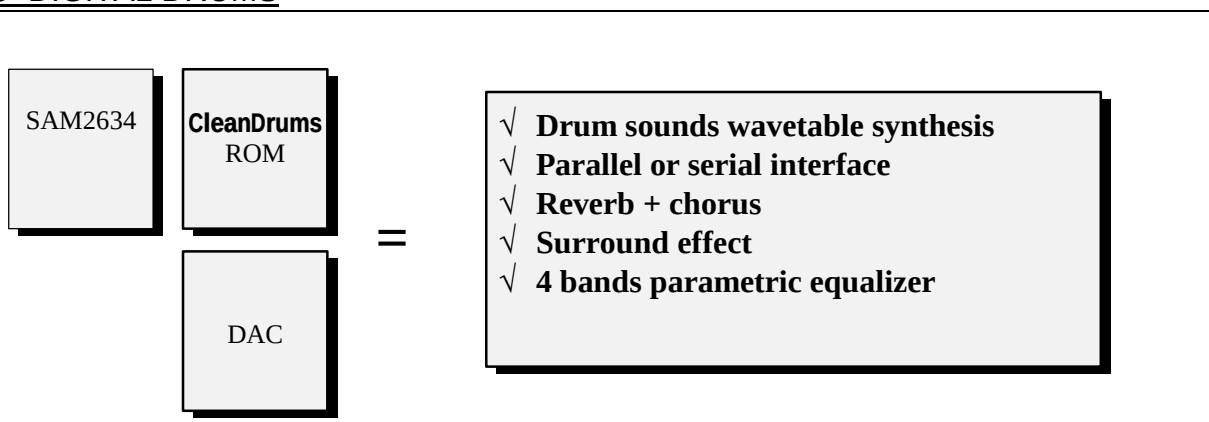
1-1- LOW COST KARAOKE, HAND-HELD KARAOKE



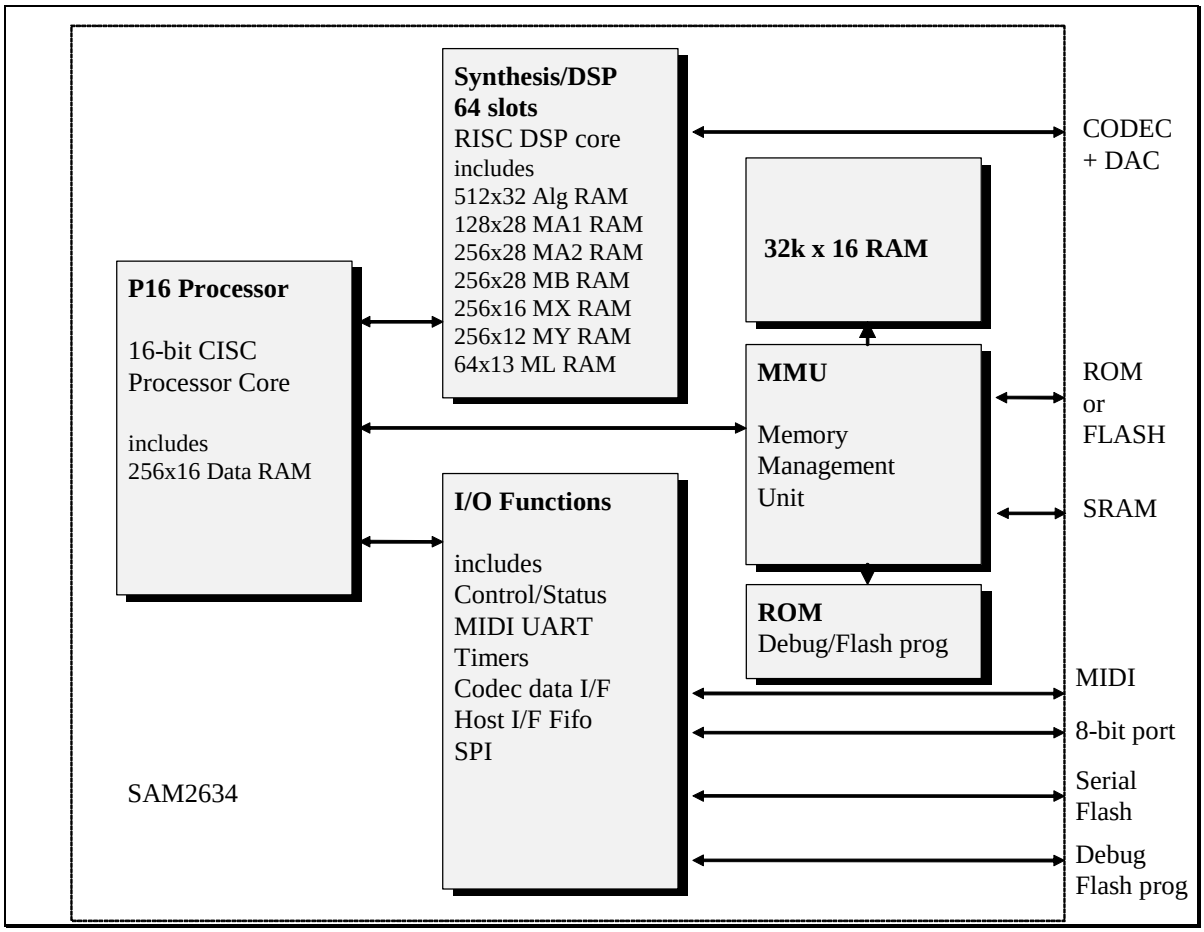
1.2 LOW COST KEYBOARD INSTRUMENT



1-3- DIGITAL DRUMS



2- GENERAL DESCRIPTION



The SAM2634 is a low cost derivative of the SAM2000 series. It retains the same high quality synthesis with up to 64 voices polyphony. The SAM2634 maximum wavetable memory is 32 MBytes and the parallel communication is through a standard 8-bit port.
The integrated 32kx16 RAM allows for high quality effects without additional component.

The highly integrated architecture from SAM2634 combines a specialized high-performance RISC-based digital signal processor (Synthesis/DSP) and a general purpose 16 bits CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the 8-bit parallel, the on-chip MIDI UART, and the Codec control interface, with minimum intervention from the control processor.

Synthesis/DSP engine

The synthesis/DSP engine operates on a frame timing basis with the frame subdivided into 64 processes slots. Each process is itself divided into 16 micro-instructions known as « algorithm ». Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be linked together to allow implementation of more complex synthesis algorithms.

A typical application will use part of the capacity of the synthesis/DSP engine for wavetable voices, another part for functions like reverb, chorus, audio in processing, surround effect, equalizer, etc. Dynamic synthesis slot allocation is possible for best polyphony/feature tradeoff.

Frequently accessed synthesis/DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM or internal 32kx16 RAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

P16 control processor and I/O functions

The Enhanced P16 control processor is the new version of P16 processor with added instructions allowing C compiling. The P16 control processor is a general purpose 16-bit CISC processor core, which runs from external memory. It includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the parallel 8-bit interface and then controls the Synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the parallel 8-bit interface through specialized « intelligent » peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The parallel 8-bit interface is implemented using one address lines (A0), a chip select signal, read and write strobes from the host and an 8-bit data bus (D0-D7).

Karaoke and keyboard applications can take advantage of the parallel 8-bit interface to communicate with the SAM2634 at high speed, with the MIDI IN and MIDI OUT signals remaining available.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM/Flash and/or internal 32kx16 RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e. internal RAM) to serve as delay lines for the synthesis/DSP and as data memory for the P16 control processor.

3- PIN DESCRIPTION

3-1- PIN BY FUNCTION – 100-pin LQFP Package

- Greyed text describes alternate function for multifunction pins.
- 5VT indicates a 5 volt tolerant Input or I/O pin.
- DR2, DR4, DR6, DR8, DR12 indicates driving capability at VOL, VOH (see § 6- D.C. CHARACTERISTICS)

Power supply group

Pin name	Pin #	Type	Decription
GND	16, 26, 33, 54, 67, 75, 95,100	PWR	Power ground - all GND pins should be returned to digital ground
VD33	15, 24, 34, 60, 74, 80, 96	PWR	Periphery power +2.7V to 3.6V. All VD33 pins should be returned to nominal +3.3V.

External PCM ROM/RAM/IO

Pin name	Pin #	Type	Decription
WA0-16	82-94, 9-12	OUT-DR6	External memory address bits, up to 2Mbit (256MByte) for direct ROM/FLASH/RAM connection.
WA17	13	OUT-DR6	External memory address bit, extension to 4Mbit
FS0	13	IN	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
WA18	14	OUT-DR6	External memory address bit, extension to 8Mbit
FS1	14	IN	Freq sense, sensed at power up. FS1|FS0 allow firmware to know operating freq of chip as follows (optional): 00b: 12 MHz @ XDIV = 0 01b: 9.6 MHz @ XDIV = 0 or 12 MHz @ XDIV = 1 10b: 11.2896 MHz @ XDIV = 0 11b: 12.288 MHz @ XDIV = 0
WA19-24	17-22	OUT-DR6	External memory address bits, extension up to 512Mbit (64MByte).
WD0-15	30-32, 35-47	I/O-DR6	External memory I/O data
WOE/	51	OUT-DR6	External memory output enable, active low
WWE/	52	OUT-DR6	External memory write enable, active low.
WCS0/	49	OUT-DR6	External ROM or FLASH chip select, active low
WCS1/	50	OUT-DR6	External RAM chip select, active low
XIO/	48	OUT-DR6	XIO/ is additional chip select for an external peripheral, active low.
CDPG/	48	OUT-DR6	CDPG/ is chip select for an external RAM used for code debug.

Serial MIDI, parallel MIDI (MPU-401)

Pin name	Pin #	Type	Decription
MIDI IN	29	IN-5VT	MIDI IN input. This pin This pin has a built-in pull up. It should be left open or tied HIGH if not used.
MIDI OUT	8	OUT-DR2	MIDI OUT output
D0-D7	53, 55-59, 61, 62	I/O -5VT-DR8	8 bit data bus to host processor.
A0	23	IN-5VT	Select address of slave 8-bit interface registers: 0: data registers (read/write) 1: status register (read) control register (write)
CS/	27	IN-5VT	Chip select from host, active low.
RD/	28	IN-5VT	Read from host, active low.
WR/	25	IN-5VT	Write from host, active low.
IRQ	81	OUT-DR4	Slave 8bit interface interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0)

Serial Peripheral Interface

Pin name	Pin #	Type	Decription
SO	68	IN-5VT	SPI serial output (from SPI device). This pin has built-in pull-down. It should be grounded or left open if not used.
SI	69	OUT-DR4	SPI serial input (to SPI device).
SCK	70	OUT-DR4	SPI serial data clock.

Digital audio group

Pin name	Pin #	Type	Decription
CKOUT	1	OUT-DR2	Buffered X2 output, can be used to drive external DAC master clock (256 * Fs)
CLBD	2	OUT-DR2	Audio data bit clock, provides timing to DABD0-1, DAAD.
WSBD	3	OUT-DR2	Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.
DABD0-DABD1	4, 5	OUT-DR2	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2x32) of serial data per frame. Audio data has up to 20 bits precision.
DAAD	6	IN-5VT	Stereo serial audio data input. This pin has built-in pull-down. It should be grounded or left open if not used.

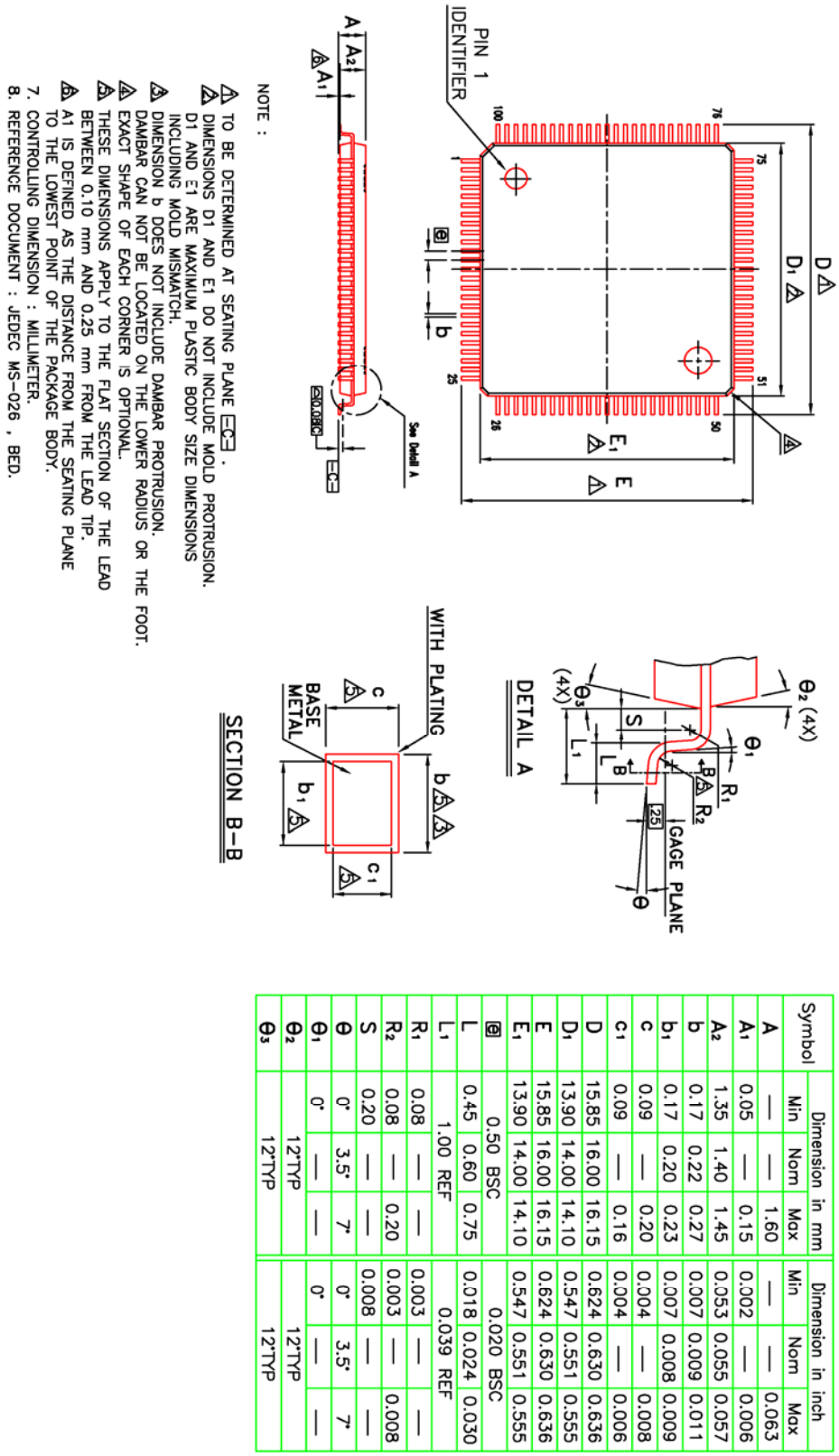
Miscellaneous group

Pin name	Pin #	Type	Decription
P0-P3	63-66	I/O -5VT-DR12	General purpose programmable I/O pins. These pins have a built-in pull down.
STIN	71	IN-5VT	Serial test input. This is a 57.6 kbaud asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	72	OUT-DR2	Serial test output. 57.6 kbauds async output used for firmware debugging.
RST/PD/	77	IN-5VT	Master reset and Power down. Schmitt trigger input. RST/PD/ should be held low during at least 10ms after power is applied. On the rising edge of RST/PD/ the chip enters its initialization routine. When RST/PD/ is low, Power-down is active: WCS0/, WCS1/, XIO/, WWE/, WOE/, MIDI_OUT, STOUT are output 1. Address and data lines are High-Z. All other outputs are set to 0. The PLL is stopped and supply voltage is removed from the core. To exit from power down, RST/PD/ must be set to VD33.
OUTVC12	73	PWR	3.3V to 1.2 V regulator output. The built-in regulator gives 1.2V for internal use only (core supply). 4.7µF or 10µF Decoupling capacitor must be connected between OUTVC12 and GND.
X1-X2	78, 79	-	External crystal connection. Standard frequencies are 12 MHz, 11.2896 MHz, 12.288 MHz. An external clock can be connected to X1. A built-in PLL multiplies the clock frequency by 4 or 3.2 for internal use.
XDIV	99	IN	System clock divider. Divide system clock by 1.25. When high, it allows using standard 12MHz Xtal for 37.5kHz sampling rate. (12MHz ÷ 1.25 ÷ 256 = 37,5kHz).
TEST	76	IN	Test pin with a built-in pull-down. It should be grounded or left open for normal operation.
NC	7, 97, 988	-	Not connected pins.

3-2- PIN-OUT BY PIN NUMBER – 100-pin LQFP Package

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	CKOUT	26	**GND**	51	WOE/	76	TEST
2	CLBD	27	CS/	52	WWE/	77	RST/PD/
3	WSBD	28	RD/	53	D0	78	X1
4	DABD0	29	MIDI_IN	54	**GND**	79	X2
5	DABD1	30	WD0	55	D1	80	**VD33**
6	DAAD	31	WD1	56	D2	81	IRQ
7	NC	32	WD2	57	D3	82	WA0
8	MIDI_OUT	33	**GND**	58	D4	83	WA1
9	WA13	34	**VD33**	59	D5	84	WA2
10	WA14	35	WD3	60	**VD33**	85	WA3
11	WA15	36	WD4	61	D6	86	WA4
12	WA16	37	WD5	62	D7	87	WA5
13	WA17-FS0	38	WD6	63	P0	88	WA6
14	WA18-FS1	39	WD7	64	P1	89	WA7
15	**VD33**	40	WD8	65	P2	90	WA8
16	**GND**	41	WD9	66	P3	91	WA9
17	WA19	42	WD10	67	**GND**	92	WA10
18	WA20	43	WD11	68	SO	93	WA11
19	WA21	44	WD12	69	SI	94	WA12
20	WA22	45	WD13	70	SCK	95	**GND**
21	WA23	46	WD14	71	STIN	96	**VD33**
22	WA24	47	WD15	72	STOUT	97	NC
23	A0	48	XIO/-CDPG/	73	OUTVC12	98	NC
24	**VD33**	49	WCS0/	74	**VD33**	99	XDIV
25	WR/	50	WCS1/	75	**GND**	100	**GND**

3-3- MECHANICAL DIMENSIONS – 100-pin LQFP Package



NOTE :

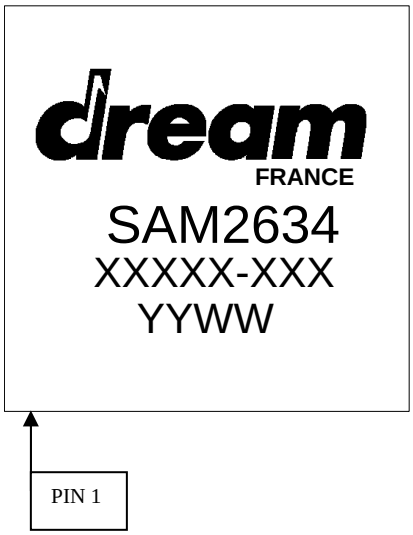
1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BED.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

ZI 21140 Semur-en-Auxois FRANCE	**TITLE:** **100LD LQFP (14 x 14 x 1.4mm)** **Package Outline -CU L/F** - L/F Material: C7025 1/2H Foot Print : 2 mm	**Package designation** LQFP100_D	**REV.** **D**

3-4- MARKING

LQFP100



4- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)*

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any 5 volt tolerant pin (5VT)	-	-0.3	-	5.5	V
Voltage on any non 5 volt tolerant pin	-	-0.3	-	VD33+0.3	V
Supply voltage	VD33	-0.3	-	3.6	V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VD33	2.7	3.3	3.6	V
Operating ambient temperature	TA	-25	-	70	°C

6- D.C. CHARACTERISTICS (TA=25°C, VD33=3.3V, X1 = 12.288MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage on 5VT pins	VIH	2	-	-	V
High level input voltage on non 5VT pins	VIH	2	-	-	V
Low level output voltage at IOL = IOHL Min	VOL	-	-	0.4	V
High level output voltage at IOH = IOHL Min	VOH	2.4	-	-	V
Schmitt-trigger negative-to-threshold voltage	VTN	0.8	1.1	-	V
Schmitt-trigger positive-to-threshold voltage	VTP	-	1.6	2	V
Driving capability at VOL, VOH for DR2 pins	IOHL	-	-	2	mA
Driving capability at VOL, VOH for DR4 pins	IOHL	-	-	4	mA
Driving capability at VOL, VOH for DR6 pins	IOHL	-	-	6	mA
Driving capability at VOL, VOH for DR8 pins	IOHL	-		8	mA
Input leakage current	IIN	-10	±1	10	µA
OUTVC12 output voltage	VD12	1.14	1.2	1.26	V
Power supply current	ID33		14		mA
Power down supply current	-		18		µA
Pull-up or Pull-down resistor	Rud	30	75	190	kOhm

7- PERIPHERALS AND TIMINGS

All timings are valid in recommended operating conditions, with load capacitance=30pF on all outputs, except X2.
All timings refer to tck, which is the internal master clock period.

- When XDIV is connected to ground, the internal master clock frequency is 4 times the frequency at pin X1. Therefore tck = txtal ÷ 4.
- When XDIV is connected to VD33, the internal master clock frequency is 3.4 times the frequency at pin X1. Therefore tck = txtal ÷ 3.4.

The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 KHz sampling rate).

7-1- CRYSTAL FREQUENCY SELECTION CONSIDERATIONS

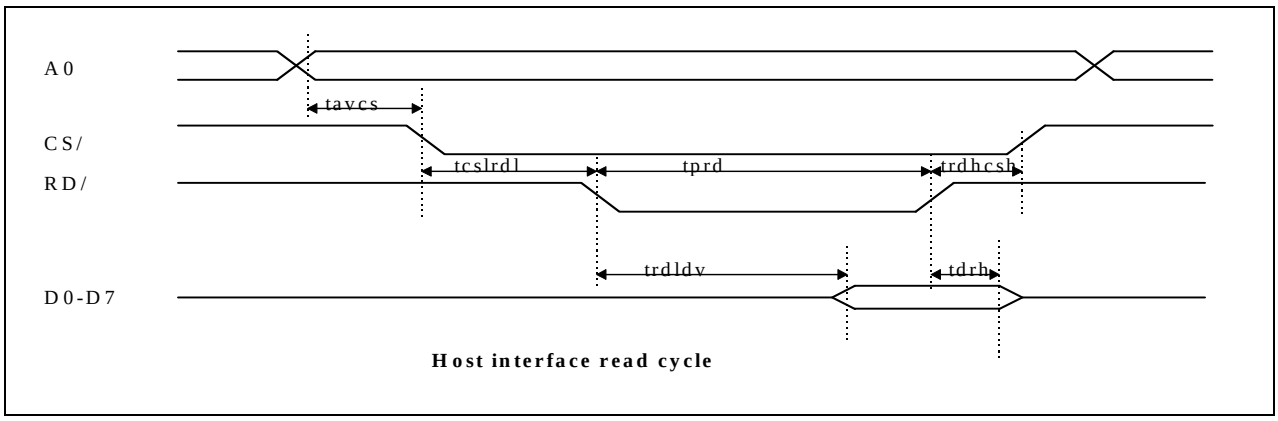
There is a trade-off between the crystal frequency and the support of widely available external ROM/Flash components. The following chart allows selecting the best fit for a given application:

Sample rate (KHz)	Xtal (MHz)	XDIV	tck (ns)	ROM tA (ns)
48	12.288	**0**	20.35	92
44.1	11.2896	0	22.14	101
37.5	12.00	1	26.04	120
37.5	9.60	0	26.04	120

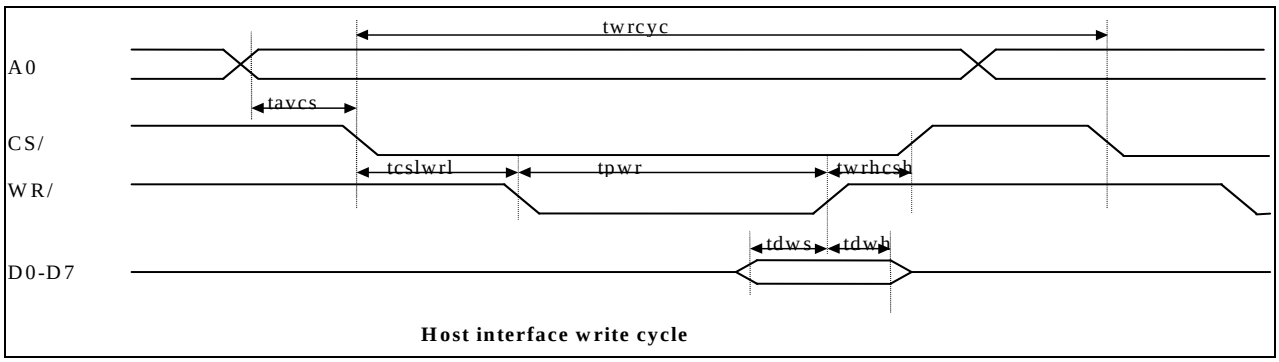
Using 12.288 MHz crystal frequency allows using widely available ROM/Flash with 90ns access time, while providing state of the art 48 KHz sampling rate

7-2- PC HOST INTERFACE

- Timings



Host interface read cycle



Host interface write cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ low	tcslrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	5	-	-	ns
RD/ pulse width	tprd	50	-	-	ns
Data out valid from RD/	trdldv	-	-	20	ns
Data out hold from RD/	tdrh	5	-	10	ns
Chip select low to WR/ low	tcslrwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	5	-	-	ns
WR/ pulse width	tpwr	50	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0	-	-	ns
Write cycle	twrcyc	128	-	-	tck

- IO Status Register

TE	RF	X	X	X	X	X	X

Status register is read when A0 = 1, RD/ = 0, CS/ = 0

TE: Transmit empty. If 0, data from SAM2634 to host is pending and IRQ is high. Reading the data at A0=0 will set TE to 1 and clear IRQ.
RF: Receiver full. If 0 then SAM2634 is ready to accept DATA from host.

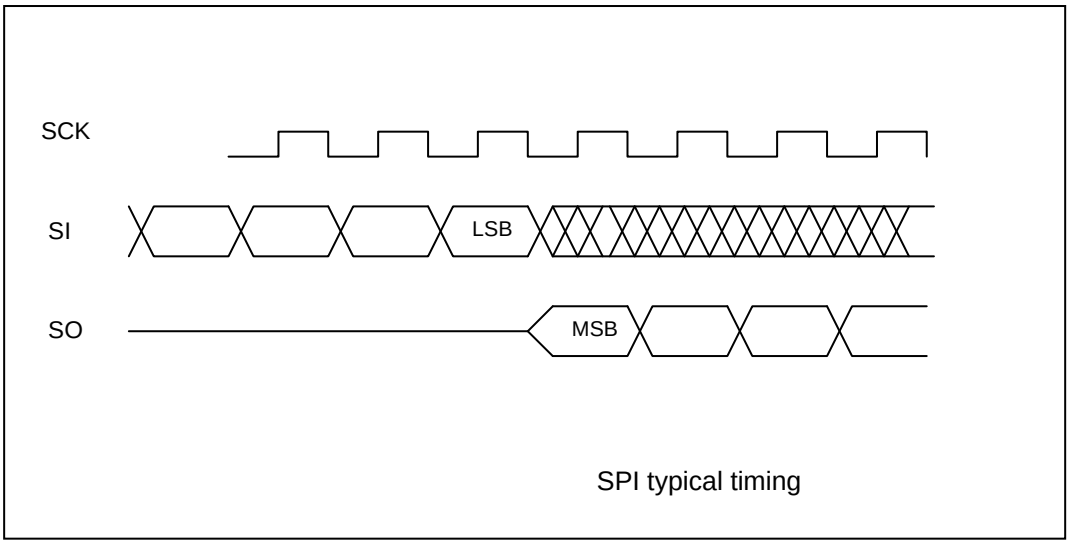
7-3- SERIAL PERIPHERAL INTERFACE

This is a master synchronous serial interface, operating in SPI mode 0.

Pins used:
SI, SCK (outputs)
SO (input)

The SCK frequency is firmware programmable from fck/4 to fck/256, fck being the system clock frequency (fck=1/tck). This allows accommodating a large variety of EEPROM/DataFlash devices.

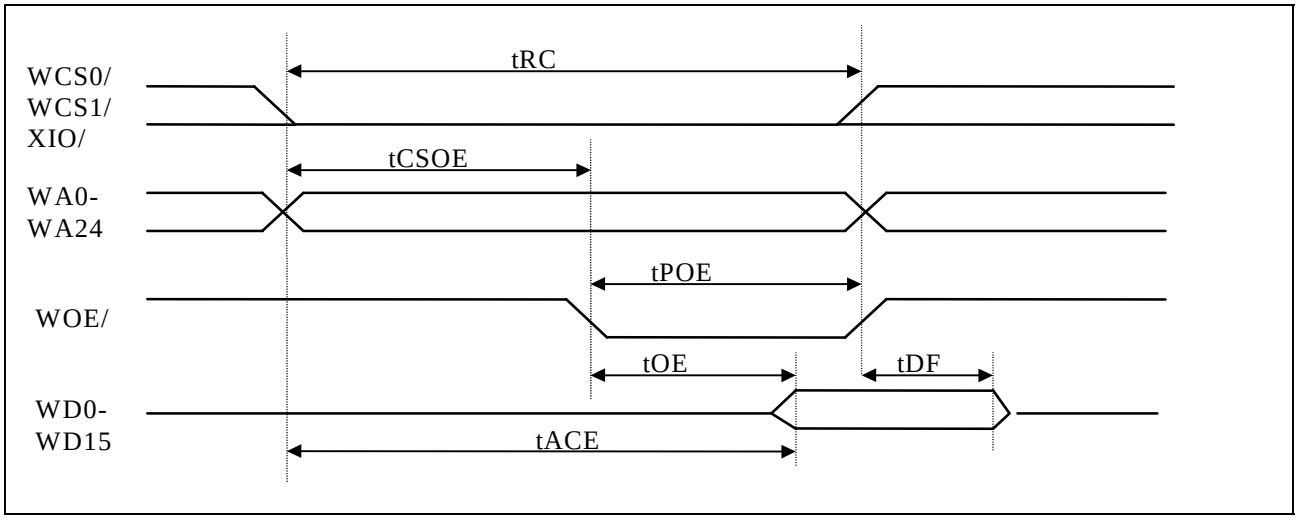
Please refer to peripheral datasheets for accurate SPI mode 0 timing.



SPI typical timing

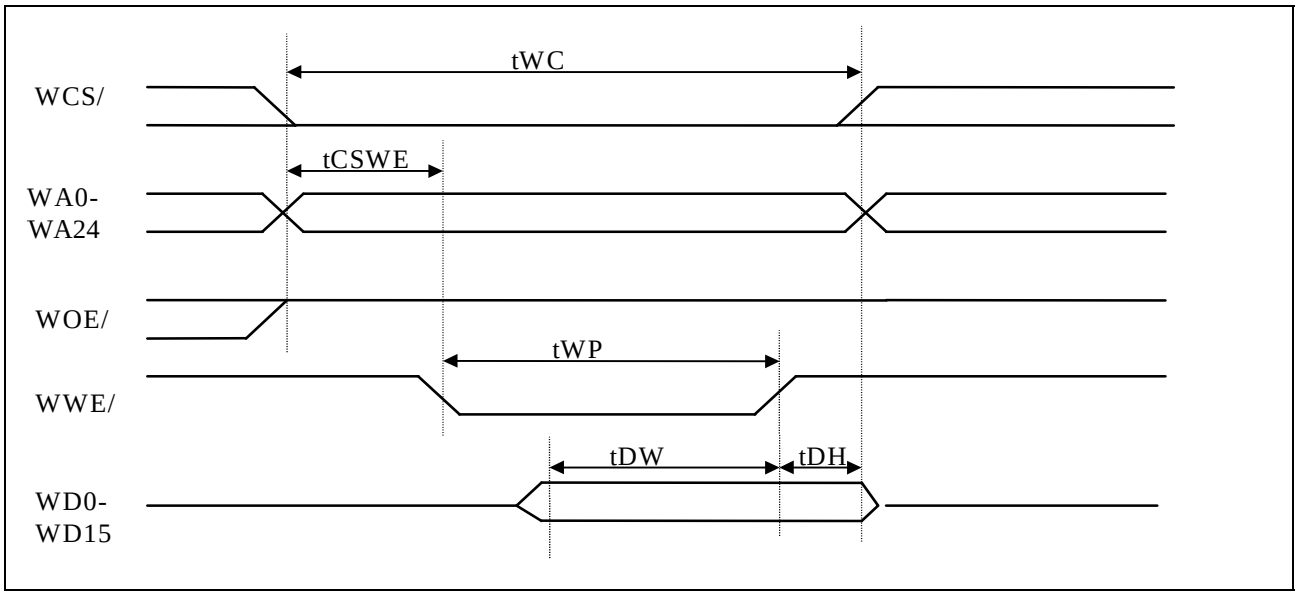
7-4- EXTERNAL ROM/Flash TIMING

ROM/Flash READ CYCLE



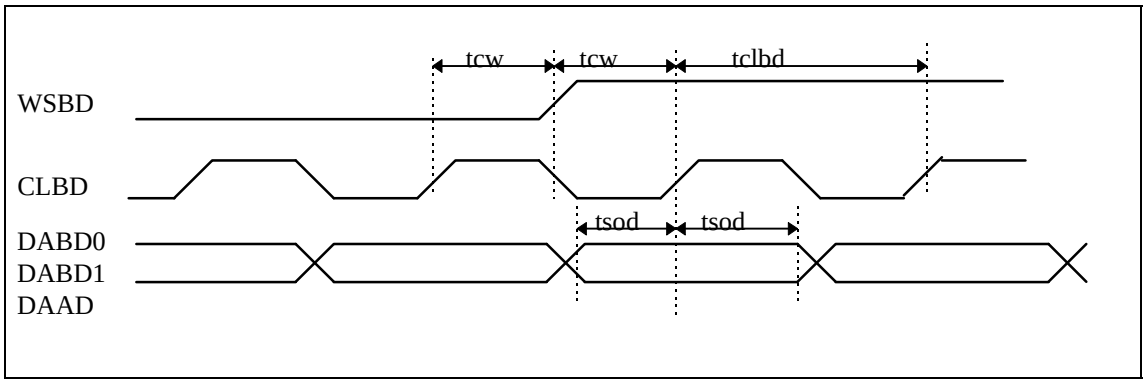
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	-	-	5*tck-10	ns
Output enable access time	tOE	-	-	5*tck-10	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	-	ns

7-5- EXTERNAL FLASH WRITE TIMING



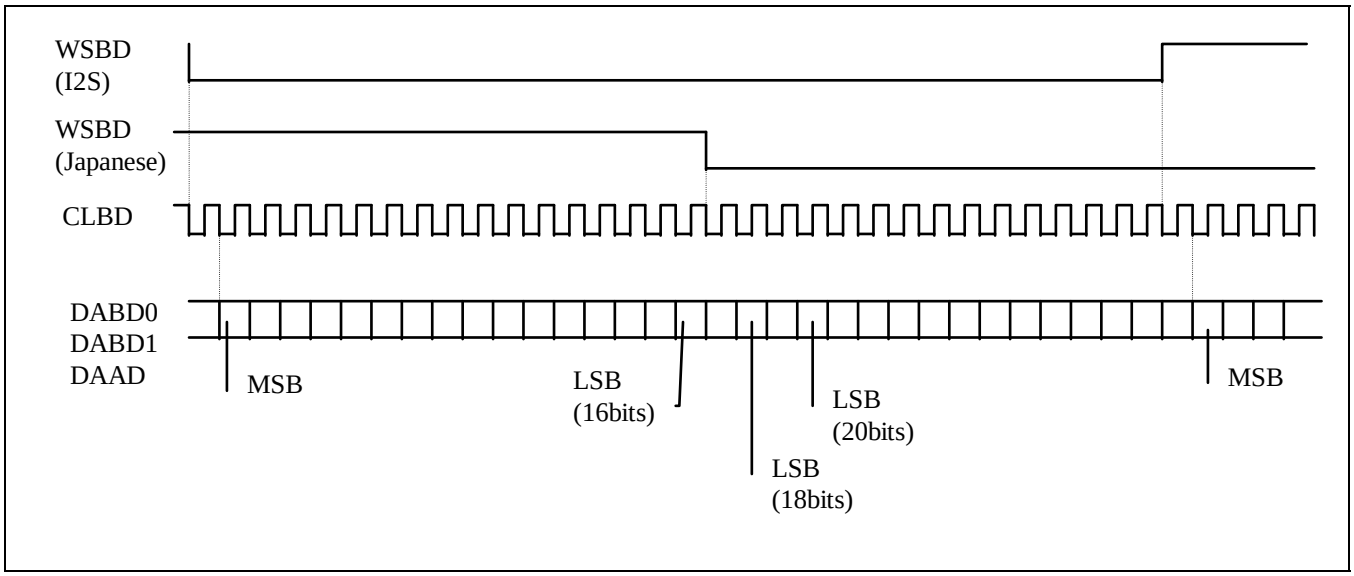
Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	tWC	5*tck	-	6*tck	ns
Write enable low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write pulse width	tWP	3*tck	3.5*tck	-	ns
Data out setup time	tDW	1.5*tck	-	-	ns
Data out hold time	tDH	5	-	-	ns

7-6- DIGITAL AUDIO TIMING



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	8*tck-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	8*tck-10	-	-	ns
CLBD cycle time	tclbd	-	16*tck	-	ns

DIGITAL AUDIO FRAME FORMAT



Notes:
- Selection between I2S and Japanese format is a firmware option
- DAAD is 16 bits only

8- RESET AND POWER DOWN

During power-up, the RST/PD/ input should be held low during 10ms. A typical RC/diode power-up network can be used.
After the low to high transition of RST/PD/, following happens:

- The Synthesis/DSP enters an idle state.
- P16 program execution starts from address 0100H in ROM space (WCS/ low).

If RST/PD/ is asserted low then the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, RST/PD/ has to be asserted high.

8-1- PIN STATUS IN POWER-DOWN

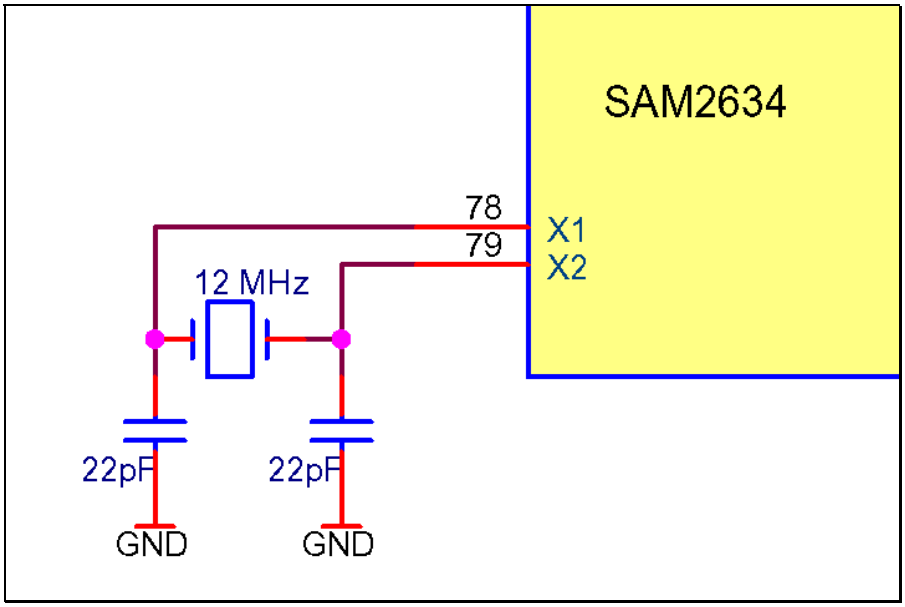
Table below shows the status of each pin in Normal mode (RST/PD/ High) and in Power-down mode (RST/PD/ Low)

Pin	Status in Normal mode	Status in Power-down mode
WA[15:0]	OUT	TRISTATE with Keeper resistor
WA[18:17]	I/O	TRISTATE with Keeper resistor
WA[24:19]	OUT	TRISTATE with Keeper resistor
WD[15:0]	I/O	IN with Keeper resistor
WOE/	OUT	TRISTATE with Pull-up resistor
WWE/	OUT	TRISTATE with Pull-up resistor
WCS0/	OUT	TRISTATE with Pull-up resistor
WCS1/	OUT	TRISTATE with Pull-up resistor
XIO/_CDPG/	OUT	TRISTATE with Pull-up resistor
MIDI IN	IN with Pull-up resistor	IN with Keeper resistor
MIDI OUT	OUT	OUT – High Level
CS/	IN	IN (floating)
RD/	IN	IN (floating)
WR/	IN	IN (floating)
IRQ	OUT	OUT – Low Level
A0	IN	IN with Keeper resistor
D[7:0]	I/O	IN (floating)
SO	IN with Pull-down resistor	IN with Keeper resistor
SI	OUT	OUT – Low Level
SCK	OUT	OUT – Low Level
CKOUT	OUT	OUT – Low Level
CLBD	OUT	OUT – Low Level
WSBD	OUT	OUT – Low Level
DABD|1:0]	OUT	OUT – Low Level
DAAD	IN with Pull-down resistor	IN with Keeper resistor
P[3:0]	I/O with Pull-down resistor	IN with Keeper resistor
STIN	IN with Pull-down resistor	IN with Keeper resistor
STOUT	OUT	OUT – High Level
RST/PD/	IN	IN driven Low
X1 – X2	Oscillator	Power-down
XDIV	IN	IN with Keeper resistor
TEST	IN with Pull-down resistor	IN with Pull-down resistor

Note:

- Keeper resistor can be pull-up or to pull-down resistor. This will depend on logic state at the pin where it is connected when switching to Power-down mode.
    - If logic state is ‘Low’ when entering Power-down mode, keeper resistor will be pull-down
    - If logic state is ‘High’ when entering Power-down mode, keeper resistor will be pull-up
- In a designs where it is planned to use the Power-down mode, external pull up or pull down resistor should be added on each pin that have the “IN (floating)” status and that is not externally driven in Power-down mode. To avoid consumption in Normal mode these resistors can have high value like 1MOhm.

9 - RECOMMENDED CRYSTAL COMPENSATION



10- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VD33, VD18 distribution, decouplings

All GND, VD33 pins should be connected. A GND plane is strongly recommended below the SAM2634. The board GND + VD33 planes could be in grid form to minimize EMI.

Recommended decoupling is 470pF in parallel with 2.2 or 4.7µF close to OUTVC12 pin. VD33 requires 0.1uF at each corner of the IC with an additional 10µFT capacitor should be placed close to the crystal.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors and the SAM2634 should be short and shielded. The ground return from the compensation capacitors should be the GND plane from SAM2634.

- Busses

Parallel layout from D0-D7 and WA0-WA23/WD0-WD15 should be avoided. The D0-D7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA24/WD0-WD15 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the D0-D7 bus, which connects both to the host and to the SAM2634 GND.

A ground plane should be implemented below the WA0-WA24/WD0-WD15 bus, which connects both to the ROM/Flash grounds and to the SAM2634.

11- PRODUCT DEVELOPPMENT AND DEBUGGING

Dream provides an integrated product development and debugging tool SamVS.
SamVS runs under Windows (XP, Vista, Win7). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program external Flash, serial Flash, EEPROM on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available such as:

- GM Synth with reverb and chorus
- MIDI functions
- File access to SD Card

Dream engineers are available to study customer specific applications.

dream

SAM2634

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