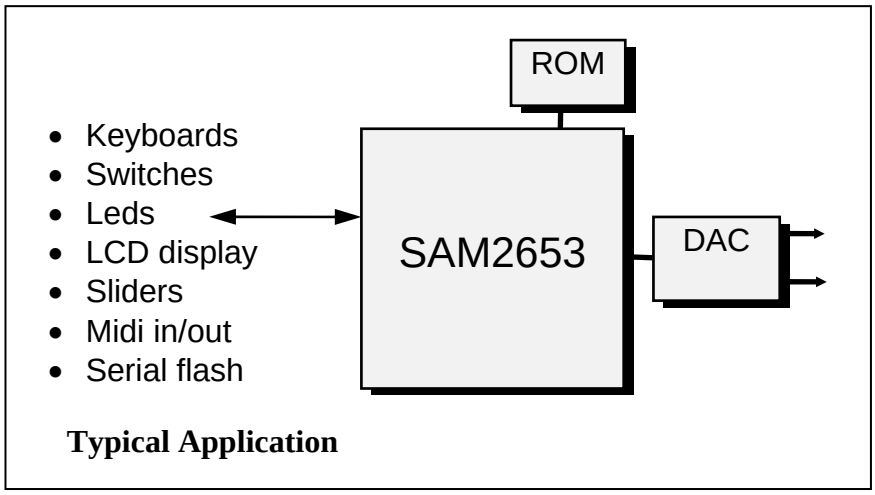
SAM2653

INTEGRATED DIGITAL MUSIC INSTRUMENT

The SAM2653 integrates into a single chip a proprietary **DREAM®** DSP core (64-slots DSP + 16-bit microcontroller), a 32k x 16 RAM, an LCD display interface and a scanner allowing direct connection to velocity sensitive keyboards, switches, LEDs, sliders. With addition of a single external ROM or FLASH, a complete low cost musical instrument can be built, including reverb and chorus effects, parametric equalizer, orchestrations, pitch bend, wheel controller, without compromising on sound quality.

Key features

- Interfaces directly to instrument hardware
  - Keyboard velocity scanner (up to 264 keys, 64 µs time accuracy, log time scale)
  - Switches scanner (up to 176 switches)
  - Led display controller (up to 88 leds)
  - Sliders scanner (built-in ADC, up to 16 sliders)
  - LCD display (8-bit interface)
- Crisp musical response
  - 49MHz built-in 16-bit micro-controller
  - Interface with keyboard / switches through built-in shared memory
- High quality sound
  - 64-slots digital sound synthesizer/processor
  - Multi-algorithm: PCM with dynamic LP filter, FM, delay lines for effects, equalizer, surround, digital audio in processing, etc.
  - Compatible with SAM25XX sounds and firmware.
  - 48 kHz sampling rate
  - Up to 64MByte ROM/Flash and RAM for firmware, orchestrations and PCM data
  - Up to 4 channels audio out, 2 channels audio in
- Top technology
  - LQFP128 Space saving package
  - Single 12.2880 MHz crystal operation, built-in PLL minimizes RFI
- Available sound banks for GM or high quality piano
  - General MIDI CleanWave® 1MByte, 4MByte and 8MByte (free license)
  - Piano 8MByte (3 variations, free license)
  - Other sample sets available under special licensing conditions
- Quick time to market
  - Enhanced P16 processor with C compiler
  - Proven reliable synthesis drivers
  - In-circuit emulation with SamVS-C debugger for easy prototype development
  - Built-in programming algorithm, allows external FLASH programming.
  - All existing SAM2000 tools available for sound and sound banks developments.



Typical Application

1- MAIN FEATURES

The SAM2653 provides a new generation of integrated solutions for electronic musical instruments. The SAM2653 includes all key circuitry into a single silicon chip: sound synthesizer/processor, 16-bit control processor, interface with keyboards, switches, sliders, leds, LCD display, etc.
The synthesis/sound processing core of the SAM2653 is taken from the SAM2000 series, whose quality has already been demonstrated through a lot of different musical products: E.Pianos, home keyboards, professional keyboards, classical organs, sound expanders. The maximum polyphony is 64 voices without effects. A typical application will be 38-voice polyphony with reverb, chorus, 4-band equalizer and surround.

The SAM2653 is directly compatible with most available musical keyboards. This includes configuration options for spring or rubber type contacts, common anode or common cathode type matrix. A 64 µs timing accuracy for velocity detection provides a very reliable dynamic response even with low cost unweighted keyboards. The time between contacts is coded with 256 steps on a logarithmic time scale, then converted by software to a 128-step MIDI scale according to the type of keyboard and a selected keyboard sensitivity.
The SAM2653 can handle directly up to 176 switches. Switches, organized in matrix form, require only a serial diode. Up to 88 leds can be directly controlled by the SAM2653 in a time multiplexed way. Additional leds can be connected through additional external shift registers using the GPIO lines (general purpose I/O) of the SAM2653. The built-in analog to digital converter of the SAM2653 allows connecting continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc. Up to 16 sliders can be connected.
The SAM2653 can be directly connected to most LCD displays through an 8-bit dedicated data bus and 3 control signals.

Configuration options allow the SAM2653 to cover a wide range of musical products, from the lowest cost keyboard to the high range digital piano, thanks to flexible memory and I/O organization: built-in 64k bytes RAM, up to 64M bytes external memory for firmware, orchestrations and PCM data. The external memory can be ROM, RAM or FLASH. Memory types can be mixed, but for most applications there is no need for external RAM memory as the built-in 64k bytes RAM is enough to handle firmware variables and reverb delay lines. External flash memory can be programmed on-board from a host processor through the SAM2653.

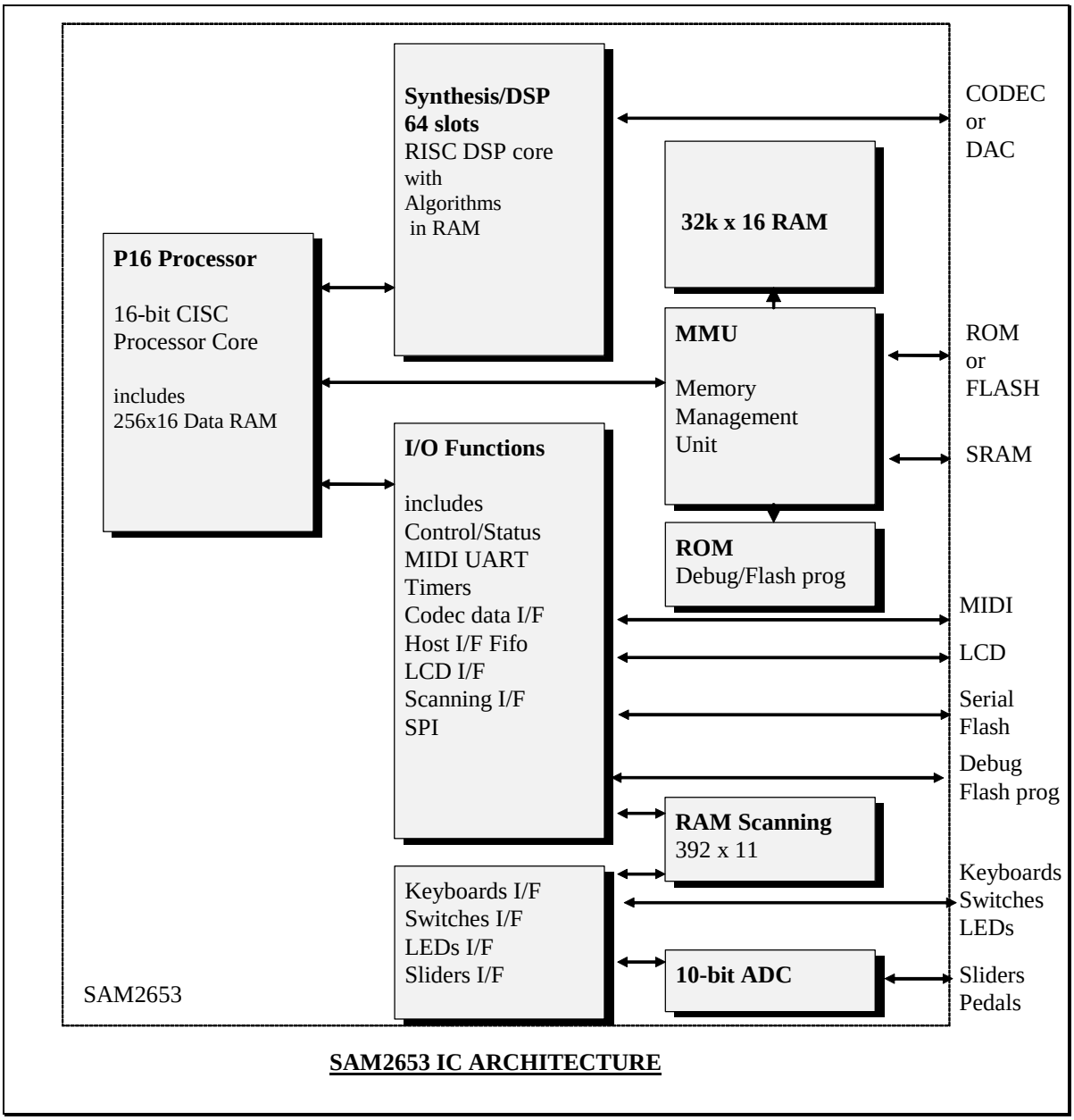
The SAM2653 operates from a single 12.2880 MHz crystal. A built-in PLL raises the frequency to 49.152MHz for internal processing. This allows to minimize radio frequency interference (RFI), making it easier to comply with FCC, CSA, CE standards.

A power-down feature is also included which can be controlled externally (RST/PD/ pin). This makes the SAM2653 very suitable for battery operated instruments.

The SAM2653 has been designed with final instrument quick time to market in mind. The SAM2653 product development program includes key features to minimize product development efforts:

- C compiler for built-in P16 processor
- Specialized debug interface, allowing on-target software development with a source code debugger.
- Standard sound generation/processing firmware
- Standard orchestration firmware
- Windows tools for sounds, sound banks and orchestrations developments
- Standard sound banks
- Strong technical support available directly from Dream

2- SAM2653 INTERNAL ARCHITECTURE



SAM2653 IC ARCHITECTURE

The highly integrated architecture from SAM2653 combines a specialized high-performance RISC-based digital signal processor (DSP) and a general purpose 16 bits CISC-based control processor (P16). An on-chip memory management unit (MMU) allows the DSP and the control processor to share an internal 32kx16 RAM as well as external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the on-chip MIDI UART and 3 timers, with minimum intervention from the control processor. A keyboard/switches/sliders/LEDs autonomous scanning interface handles the specific music instrument peripherals, including accurate keyboard velocity detection and communicates with the control processor through a dedicated 392x11 dual port RAM. An LCD display interface allows direct connection to common LCD displays

DSP engine

The DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as « algorithm ». Up to 32 DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications.

The DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical musical instrument application will use a little more than half the capacity of the DSP engine for synthesis, thus providing state of the art 38 voices synthesis polyphony. The remaining processing power may be used for typical function like reverberation, chorus, surround effect, equalizer, etc.

Frequently accessed DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM, or into the built-in 32kx16 RAM. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20.3 ns (49 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 294 million operations per second (MOPS).

Enhanced P16 control processor and I/O functions

The Enhanced P16 control processor is the new version of P16 processor with added instructions allowing C compiling. The P16 is a general-purpose 16-bit CISC processor core, which runs from external memory. A debug ROM is included on-chip for easy development of firmware directly on the target system. This ROM also contains the necessary code to directly program externally connected flash memory. The P16 includes 256 words of local RAM data memory for use as registers, scratchpad data and stack.

The P16 control processor writes to the parameter RAM blocks within the DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the scanning interface and then controls the DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the scanning interface through specialized « intelligent » peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single ROM device to serve as sample memory storage for the DSP and as program storage for the P16 control processor. An internal 32kx16 RAM is also connected to the MMU, allowing RAM resources to be shared between the DSP for delay lines and the P16 for program data.

Keyboards/Switches/Sliders/LEDs scanning interface

The scanning interface consists of hardwired logic. It time multiplexes keyboard, switches and LEDs connections therefore minimizing the amount of wiring required. It communicates with the P16 through a 392x11 dual port RAM and a few control registers. When a new incoming event is detected, such as key-on, key-off or switch change, the scanning interface will notify the P16 by indicating the type of event. The P16 then simply reads the dual port RAM to get the corresponding parameter, such as velocity or switch status. Conversely, the P16 simply writes into the dual port RAM the LED states to be displayed and the scanning interface will then take care of time multiplexing the display.
The scanning interface uses an unique key velocity detect scheme with a pseudo-logarithmic time scale. This allows velocities to be accurately detected, even when keyboard keys are pressed very softly.

Finally a built-in 10-bit analog to digital converter (ADC) allows the connection of up to 16 continuous controllers through external analog multiplexers such as the 4051.

LCD display interface

The LCD display interface uses a dedicated bidirectional data bus (DB0-DB7) an Instruction/data control RS, a read write signal R/W and an enable signal ENB. Built-in features are included to accommodate even the slowest LCD displays.

Flash programming

The SAM2653 enables to program flash memories on three different ways:

- Blank flash programming is done by the debug interface. This mode is very slow and should be reserved for the initial boot sector programming
- Program update. All the flash content can be re-programmed. The SAM2653 cannot play music during the flash erase and programming. A specific firmware is used to program flash with the DSP
- Parameters update, e.g. in keyboard applications, backup parameter and sequencer song. If the flash enables concurrent read while program/erase, it is possible to backup parameters in the upper memory plane while the µp firmware is running on the lower plane. The SAM2653 cannot play music during the parameter backup because sound samples are stored in both memory planes.

Flash feature

- 3.3v or 5v
- Access time: 90 ns (for 12.288 MHz crystal)

3- PIN DESCRIPTION

3-1- PINS BY FUNCTION – 128-pin LQFP Package

- Greyed text describes alternate function for multifunction pins.
- 5VT indicates a 5 volt tolerant Input or I/O pin.
- DR2, DR4, DR6, DR8, DR12 indicates driving capability at VOL, VOH (see § 6- D.C. CHARACTERISTICS)

Power supply group

Pin name	Pin #	Type	Description
GND	17, 32, 49, 70, 83, 95, 114, 128	PWR	DIGITAL GROUND All pins should be connected to a ground plane
AGND	92	PWR	ANALOG GROUND for the ADC. Should be connected to a clean analog ground.
VD33	16, 29, 50, 76, 94, 100, 116	PWR	POWER SUPPLY, +3.3V nominal (2.7V - 3,6V). All pins should be connected to a VD33 plane
VA33	91	PWR	Analog power for the ADC, +3.3V nominal (2.7V - 3,6V).

External PCM ROM/RAM/IO

Pin name	Pin #	Type	Description
WA0-WA16	101-113, 10-13	OUT-DR6	External memory address bits, up to 2Mbit (256kByte) for direct ROM/FLASH/RAM connection.
WA17	14	OUT-DR6	External memory address bit, extension to 4Mbit
FS0	14	IN	Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1)
WA18	15	OUT-DR6	External memory address bit, extension to 8Mbit
FS1	15	IN	Freq sense, sensed at power up. FS1|FS0 allow firmware to know operating freq of chip as follows (optional): 00b: 12 MHz @ XDIV = 0 01b: 9.6 MHz @ XDIV = 0 or 12 MHz @ XDIV = 1 10b: 11.2896 MHz @ XDIV = 0 11b: 12.288 MHz @ XDIV = 0
WA19-WA24	18-23	OUT-DR6	External memory address bits, extension up to 512Mbit (64MByte x 16).
WD0-WD15	46-48, 51-63	I/O-DR6	External memory I/O data.
WOE/	67	OUT-DR6	External memory output enable, active low.
WWE/	68	OUT-DR6	External memory write enable, active low.
WCS0/	65	OUT-DR6	External ROM or FLASH chip select, active low.
WCS1/	66	OUT-DR6	External RAM chip select, active low.
XIO/	64	OUT-DR6	XIO/ is additional chip select for an external peripheral.
CDPG/	64	OUT-DR6	CDPG/ is chip select for an external RAM used for code debug.

Serial MIDI

Pin name	Pin #	Type	Description
MIDI_IN	42	IN-5VT	Serial MIDI IN. This pin This pin has a built-in pull up. It should be left open or tied HIGH if not used.
MIDI_OUT	9	OUT-DR6	Serial MIDI OUT

Keyboard, switches, leds, sliders scanning

Pin name	Pin #	Type	Description
KBDIO/	84	OUT-DR2 Open Drain	If 1, BR[0-10] & MK[0-10] hold keyboard contact input data. If 0, BR[0-10] hold switch status input, MK[0-10] hold led data output. This output is open drain type to allow direct drive of external +5V scanning logic . It should be pulled up externally by 1k pull-up resistor.
ROW0-ROW3	24-27	OUT-DR2 Open Drain	Row select: keyboard, switches/leds, external slider analog multiplexer (4051) channel select. Sixteen rows combined with eleven BR/MK columns allow to control 176 keys, 176 switches, 88 leds and 16 sliders. These outputs are open drain type to allow direct drive of external +5V scanning logic. They should be pulled up externally by 1k pull-up resistor.
BR0-BR10	28, 30, 33-41	IN-5VT	Kbd contact 1 / switch status. When KBDIO/=1 then BR[0-10] hold the keyboard key-off or first contact status. This can be configured as normally close (spring type), normally open (rubber type), common anode or common cathode contact diodes. When KBDIO/=0 then BR[0-10] hold the switch status from ROW[0-4]
MK0-MK10	115, 117-126	I/O -5VT-DR8	Kbd contact 2 / led data. When KBDIO/=1 then MK[0-10] hold the keyboard key-on or second contact status. This can be configured as common anode or common cathode contact diodes. When KBDIO/=0 then MK[0-10] hold the led data from ROW[0-4]
VIN	90	ANA	Slider analog input. Ranges from AGND to VA33. Should hold the ROW[0-3] slider voltage. Multiple sliders should be connected through external analog multiplexer(s) like 4051.

LCD Display Interface

The following signals are controlled by firmware, therefore their timing relationship is determined by firmware only.

Pin name	Pin #	Type	Description
RS	44	OUT-DR8	Select Instruction (LOW) or Data (HIGH)
RW	45	OUT-DR8	Select Write (LOW) or Read (HIGH)
ENB	43	OUT-DR8	Enable, active high
DB0-DB7	69, 71-75, 77, 78	I/O -5VT-DR6	Bi-directional data bus

Serial Peripheral Interface

Pin name	Pin #	Type	Description
SO	85	IN-5VT	SPI serial output (from SPI device). This pin has built-in pull-down. It should be grounded or left open if not used.
SI	86	OUT-DR4	SPI serial input (to SPI device)
SCK	87	OUT-DR4	SPI serial data clock

Digital audio group

Pin name	Pin #	Type	Description
CKOUT	3	OUT-DR2	External DAC/Codec master clock (256 x Fs)
CLBD	4	OUT-DR2	Digital audio bit clock
WSBD	5	OUT-DR2	Digital audio left/right select
DABD0-DABD1	6, 7	OUT-DR2	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2x32) of serial data per frame. Audio data has up to 20 bits precision.
DAAD	8	IN-5VT	Stereo serial audio data input. This pin has built-in pull-down. It should be grounded or left open if not used.

Miscellaneous group

Pin name	Pin #	Type	Description
P0	79	I/O -5VT-DR8	General purpose programmable I/O pin. This pin has a built-in pull down.
ROW4	79	OUT-DR8	Additional ROW4 allows using keyboards with other matrix than 8*11 (e.g. 22*4) or multiple keyboards up to 264 keys.
P1-P3	80-82	I/O -5VT-DR12	General purpose programmable I/O pins. These pins have a built-in pull down.
STIN	88	IN-5VT	Serial test input. This is a 57.6 kbaud asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation.
STOUT	89	OUT-DR2	Serial test output. 57.6 kbauds async output used for firmware debugging.
RST/PD/	97	IN-5VT	Master reset and Power down. Schmitt trigger input with pull-up. RST/PD/ should be held low during at least 10ms after power is applied. On the rising edge of RST/PD/ the chip enters its initialization routine. When RST/PD/ is low, Power-down is active
OUTVC12	93	PWR	3.3V to 1.2 V regulator output. The built-in regulator gives 1.2V for internal use only (core supply). 4.7µF or 10µF decoupling capacitors must be connected between OUTVC12 and GND.
X1-X2	98,99	-	External crystal connection. Standard frequencies are 12 MHz, 11.2896 MHz, 12.288 MHz. An external clock can be connected to X1. A built-in PLL multiplies the clock frequency by 4 or 3.2 for internal use.
XDIV	127	IN	System clock divider. Divide system clock by 1.25. When high, it allows using standard 12MHz Xtal for 37.5kHz sampling rate. (12MHz ÷ 1.25 ÷ 256 = 37,5kHz).
TEST	96	IN	Test pin with a built-in pull-down. It should be grounded or left open for normal operation.
NC	1, 2, 31	-	Not Connected pins

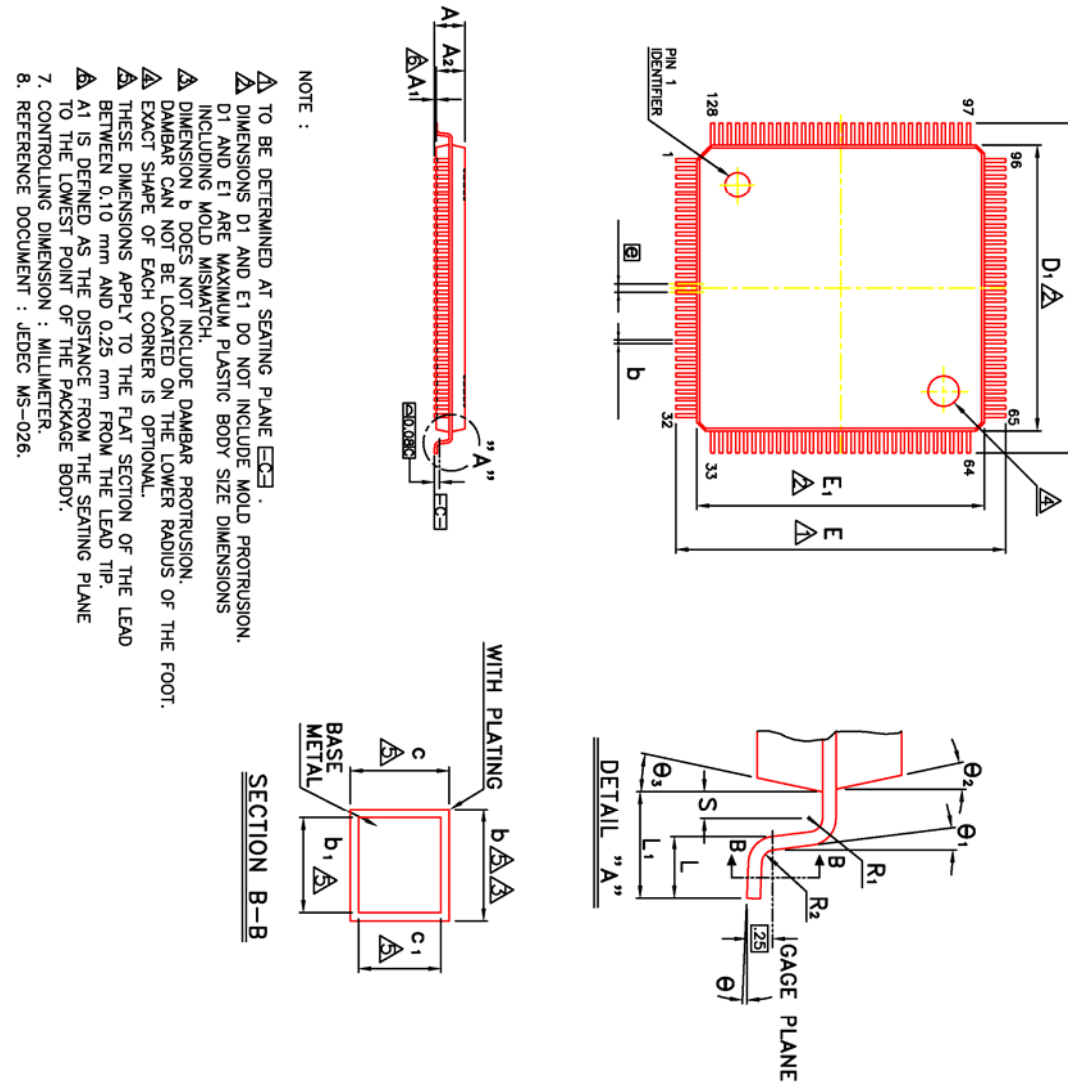
3-2- PIN-OUT BY PIN# – 128-pin LQFP Package

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	NC	33	BR2	65	WCS0/	97	RST/PD/
2	NC	34	BR3	66	WCS1/	98	X1
3	CKOUT	35	BR4	67	WOE/	99	X2
4	CLBD	36	BR5	68	WWE/	100	**VD33**
5	WSBD	37	BR6	69	DB0	101	WA0
6	DABD0	38	BR7	70	**GND**	102	WA1
7	DABD1	39	BR8	71	DB1	103	WA2
8	DAAD	40	BR9	72	DB2	104	WA3
9	MIDI_OUT	41	BR10	73	DB3	105	WA4
10	WA13	42	MIDI_IN	74	DB4	106	WA5
11	WA14	43	ENB	75	DB5	107	WA6
12	WA15	44	RS	76	**VD33**	108	WA7
13	WA16	45	RW	77	DB6	109	WA8
14	WA17-FS0	46	WD0	78	DB7	110	WA9
15	WA18-FS1	47	WD1	79	P0-ROW4	111	WA10
16	**VD33**	48	WD2	80	P1	112	WA11
17	**GND**	49	**GND**	81	P2	113	WA12
18	WA19	50	**VD33**	82	P3	114	**GND**
19	WA20	51	WD3	83	**GND**	115	MK0
20	WA21	52	WD4	84	KBDIO/	116	**VD33**
21	WA22	53	WD5	85	SO	117	MK1
22	WA23	54	WD6	86	SI	118	MK2
23	WA24	55	WD7	87	SCK	119	MK3
24	ROW0	56	WD8	88	STIN	120	MK4
25	ROW1	57	WD9	89	STOUT	121	MK5
26	ROW2	58	WD10	90	VIN	122	MK6
27	ROW3	59	WD11	91	**VA33**	123	MK7
28	BR0	60	WD12	92	**AGND**	124	MK8
29	**VD33**	61	WD13	93	OUTVC12	125	MK9
30	BR1	62	WD14	94	**VD33**	126	MK10
31	NC	63	WD15	95	**GND**	127	XDIV
32	**GND**	64	XIO/-CDPG/	96	TEST	128	**GND**

3-3- MARKING

LQFP128

3-4- MECHANICAL DIMENSIONS – 128-pin LQFP Package



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	12°TYP			12°TYP		
θ_3	12°TYP			12°TYP		

ZI 21140 Semur-en-Auxois FRANCE	**TITLE:** **128LD LQFP (14 x 14 x 1.4mm)** **Package Outline -CU L/F** - L/F Material: C7025 1/2H - Foot Print : 2 mm	**Package designation** LQFP128_A	**REV.** **A**

4- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)*

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any 5 volt tolerant pin (5VT)	-	-0.3	-	5.5	V
Voltage on any non-5 volt tolerant pin	-	-0.3	-	VD33+0.3	V
Supply voltage	VD33	-0.3	-	3.6	V
Supply voltage	VA33	-0.3	-	3.6	V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Digital supply voltage	VD33	2.7	3.3	3.6	V
Analog supply voltage (ADC)	VA33	2.7	3.3	3.6	V
Operating ambient temperature	TA	-25	-	70	°C

6- D.C. CHARACTERISTICS (TA=25°C, VD33=3.3V TA=25°C, VD33=3.3V, X1=12.288MHz)

6-1- GENERAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage on 5VT pins	VIH	2	-	-	V
High level input voltage on non 5VT pins	VIH	2	-	-	V
Low level output voltage at IOL = IOHL Min	VOL	-	-	0.4	V
High level output voltage at IOH = IOHL Min	VOH	2.4	-	-	V
Schmitt-trigger negative-to-threshold voltage	VTN	0.8	1.1	-	V
Schmitt-trigger positive-to-threshold voltage	VTP	-	1.6	2	V
Driving capability at VOL, VOH for DR2 pins	IOHL	-	-	2	mA
Driving capability at VOL, VOH for DR4 pins	IOHL	-	-	4	mA
Driving capability at VOL, VOH for DR6 pins	IOHL	-	-	6	mA
Driving capability at VOL, VOH for DR8 pins	IOHL	-		8	mA
Driving capability at VOL, VOH for DR12 pins	IOHL	-		12	mA
Input leakage current	IIN	-10	±1	10	µA
OUTVC12 output voltage	VD12	1.14	1.2	1.26	V
Power supply current	ID33		35		mA
Power down supply current	-		18		µA
Pull-up, Pull-down or Keeper resistor	Rudk	30	75	190	kOhm

7- PERIPHERALS AND TIMINGS

All timings are valid in recommended operating conditions, with load capacitance=30pF on all outputs, except X2.
All timings refer to tck, which is the internal master clock period.

- When XDIV is connected to ground, the internal master clock frequency is 4 times the frequency at pin X1. Therefore tck = txtal ÷ 4.
- When XDIV is connected to VD33, the internal master clock frequency is 3.4 times the frequency at pin X1. Therefore tck = txtal ÷ 3.4.

The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 KHz sampling rate).

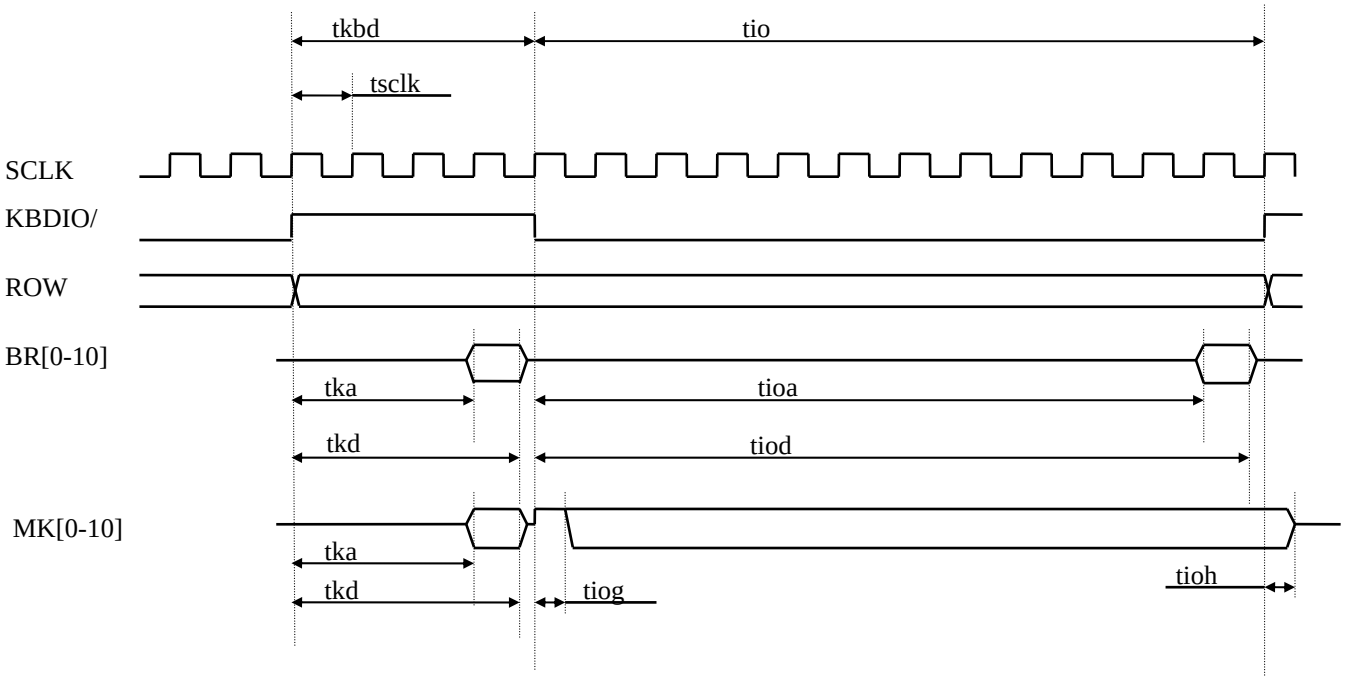
7-1- CRYSTAL FREQUENCY SELECTION CONSIDERATIONS

There is a trade-off between the crystal frequency and the support of widely available external ROM/Flash components. The following chart allows selecting the best fit for a given application:

Sample rate (KHz)	Xtal (MHz)	XDIV	tck (ns)	ROM tA (ns)	COMMENT
48	**12.288**	**0**	**20.35**	**92**	**Recommended for current designs**
44.1	11.2896	0	22.14	101	
37.5	12.00	1	26.04	120	
46.875	12.00	0	20.83	95	

Using 12.288 MHz crystal frequency allows using widely available ROM/Flash with 90ns access time, while providing state of the art 48 KHz sampling rate

7-2- SCANNING (KEYBOARD, SWITCHES, LEDS, SLIDERS)



Conditions: 12.288 MHz Xtal, scanning clock divide factor = 1 (See ProgRef26x3)

Parameter	Symbol	Min	Typ	Max	Unit
Keyboard access (KBDIO/ high time)	Tkbd		1.3		µs
Switches/leds access (KBDIO/ low time)	Tio		3.9		µs
Internal scanning clock period	Tsclk		325		ns
Break (contact1) and Make (contact2) data from Keyboard valid from rising KBDIO/	Tka			1.1	µs
Break (contact1) and Make (contact2) data from Keyboard floating from rising KBDIO/	tkd	1.2		1.5	µs
Switch data valid from falling KBDIO/	tioa			3.6	µs
Switch data floating from falling KBDIO/	tiod	3.7		4	µs
Led data MK guard time	tiog	27		163	ns
Led data floating from rising KBDIO/	tioh	0		82	ns

Note:
- if scanning clock divide factor = 2, scanning timings should be multiplied by 2
- if scanning clock divide factor = 4, scanning timings should be multiplied by 4

7-3-LCD DISPLAY INTERFACE

Pin used: DB8-DB0 (I/O), RS (output), RW (output), ENB (output).
The SAM2653 can be directly connected to most LCD display
All signals are controlled by P16 firmware, therefore their timing relationship is determined by firmware only

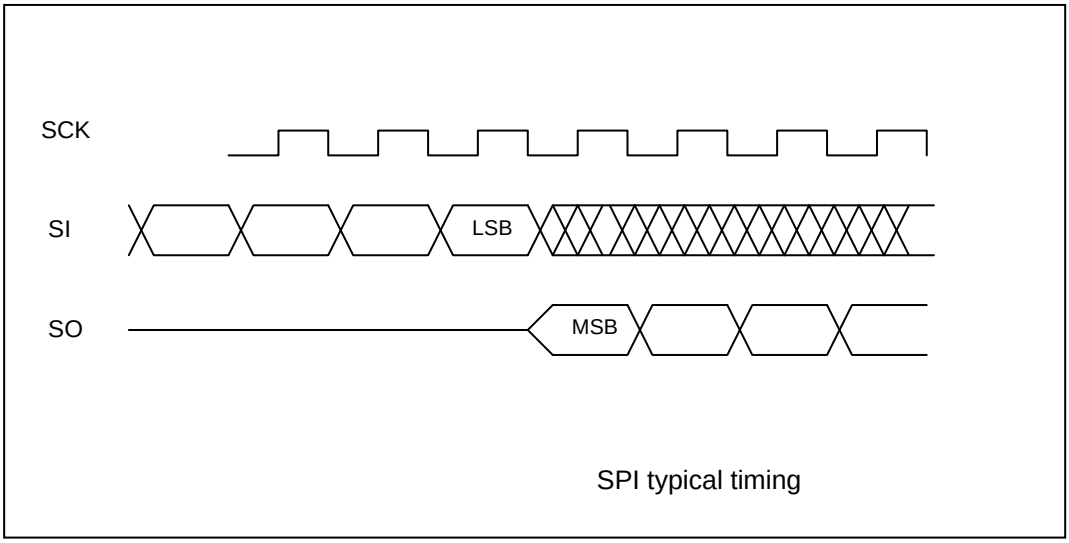
7-4- SERIAL PERIPHERAL INTERFACE

This is a master synchronous serial interface, operating in SPI mode 0.

Pins used:
SI, SCK (outputs)
SO (input)

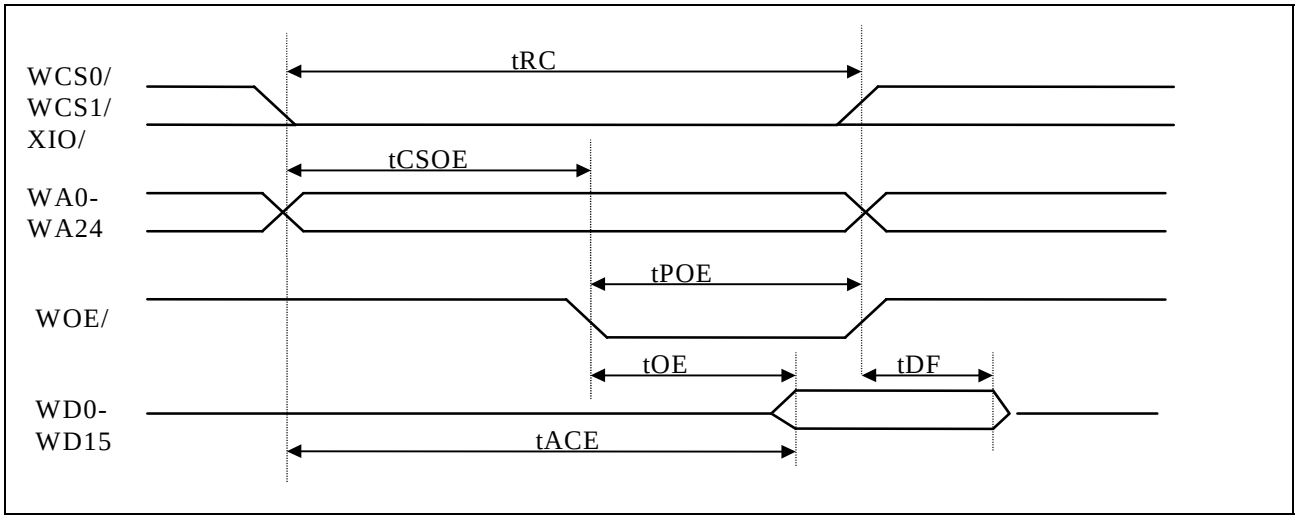
The SCK frequency is firmware programmable from fck/4 to fck/256, fck being the system clock frequency (fck=1/tck). This allows accommodating a large variety of EEPROM/DataFlash devices.

Please refer to peripheral datasheets for accurate SPI mode 0 timing.



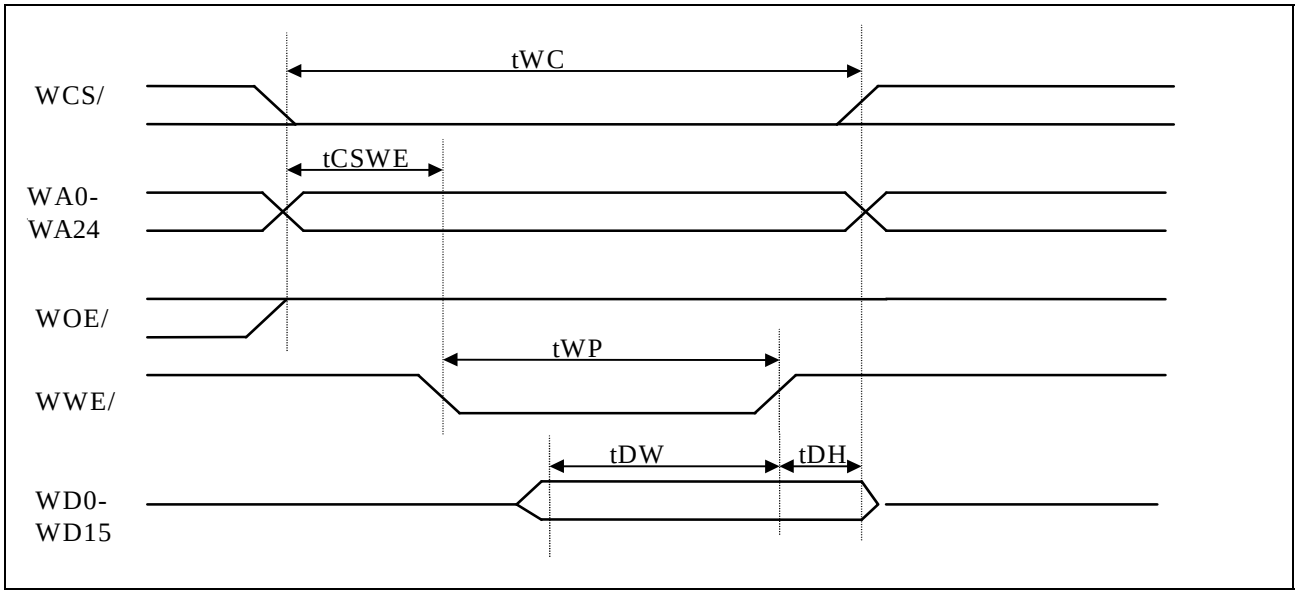
SPI typical timing

7-5- External ROM/Flash, RAM, I/O read timing



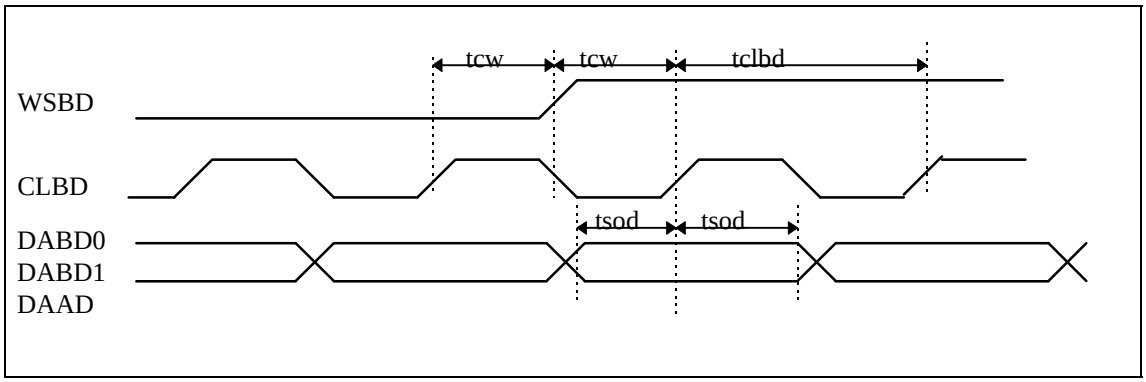
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	-	-	5*tck-10	ns
Output enable access time	tOE	-	-	3*tck-10	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	-	ns

7-6- External Flash, RAM, I/O write timing



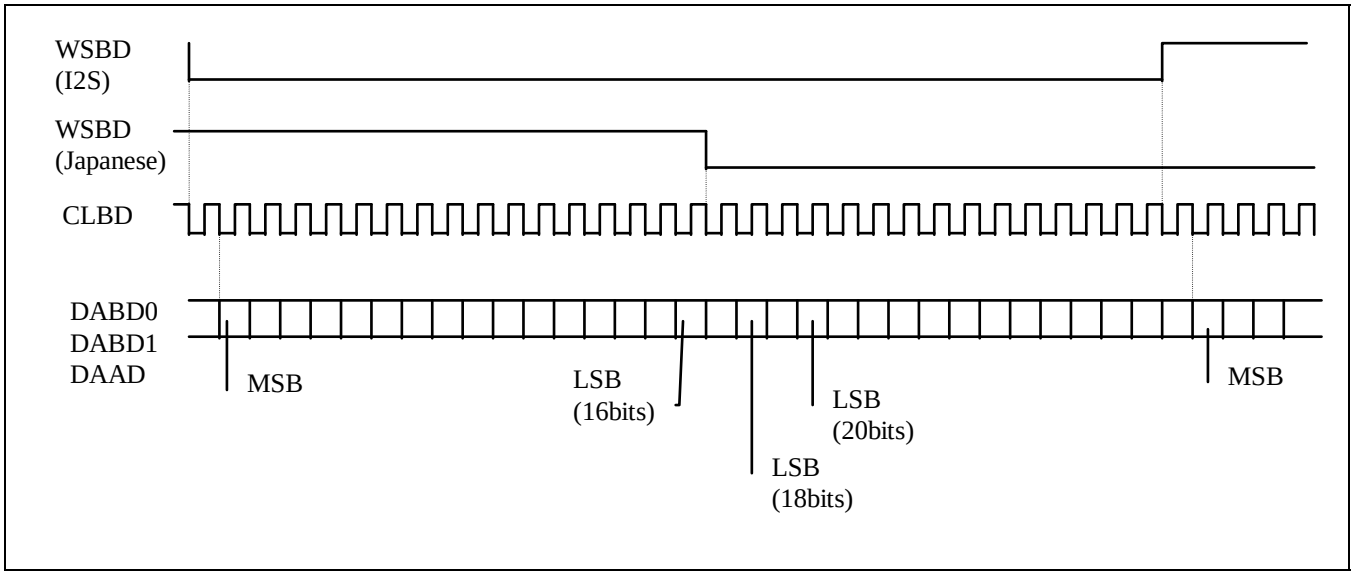
Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	tWC	5*tck	-	6*tck	ns
Write enable low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write pulse width	tWP	3*tck	3.5*tck	-	ns
Data out setup time	tDW	1.5*tck	-	-	ns
Data out hold time	tDH	5	-	-	ns

7-7- DIGITAL AUDIO



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	8*tck-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	8*tck-10	-	-	ns
CLBD cycle time	tclbd	-	16*tck	-	ns

Digital audio frame format



8- RESET AND POWER DOWN

During power-up, the RST/PD/ input should be held low during 10ms. A typical RC/diode power-up network can be used.
After the low to high transition of RST/PD/, following happens:

- The Synthesis/DSP enters an idle state.
- P16 program execution starts from address 0100H in ROM space (WCS/ low).

If RST/PD/ is asserted low then the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode, as power is removed from the core.
To exit power down, RST/PD/ has to be asserted high.

8-1- PIN STATUS IN POWER-DOWN

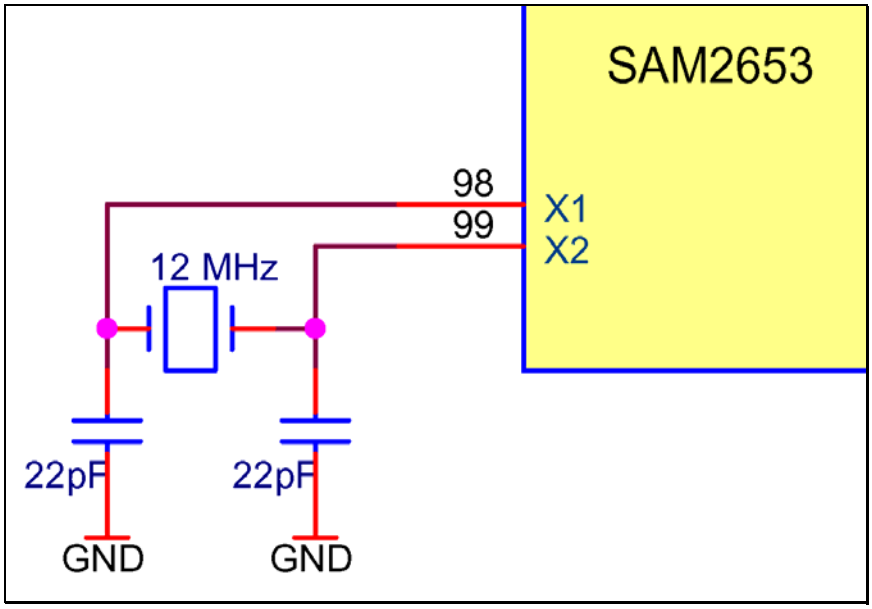
Table below shows the status of each pin in Normal mode (RST/PD/ High) and in Power-down mode (RST/PD/ Low)

Pin	Status in Normal mode	Status in Power-down mode
WA[15:0]	OUT	TRISTATE with Keeper resistor
WA[18:17]	I/O	TRISTATE with Keeper resistor
WA[24:19]	OUT	TRISTATE with Keeper resistor
WD[15:0]	I/O	IN with Keeper resistor
WOE/	OUT	TRISTATE with Pull-up resistor
WWE/	OUT	TRISTATE with Pull-up resistor
WCS0/	OUT	TRISTATE with Pull-up resistor
WCS1/	OUT	TRISTATE with Pull-up resistor
XIO/_CDPG/	OUT	TRISTATE with Pull-up resistor
MIDI IN	IN with Pull-up resistor	IN with Keeper resistor
MIDI OUT	OUT	OUT – High Level
KBDIO/	OUT	TRISTATE
ROW[3:0]	OUT	TRISTATE
BR[3:0]	IN	IN (floating)
BR[10:0]	IN	IN with Keeper resistor
MK[10:0]	I/O	IN with Keeper resistor
VIN	ANA IN	ANA IN
RS	OUT	OUT – Low Level
RW	OUT	OUT – Low Level
ENB	OUT	OUT– Low Level
DB[7:0]	I/O	IN (floating)
SO	IN with Pull-down resistor	IN with Keeper resistor
SI	OUT	OUT – Low Level
SCK	OUT	OUT – Low Level
CKOUT	OUT	OUT – Low Level
CLBD	OUT	OUT – Low Level
WSBD	OUT	OUT – Low Level
DABD|1:0]	OUT	OUT – Low Level
DAAD	IN with Pull-down resistor	IN with Keeper resistor
P[3:0]	I/O with Pull-down resistor	IN with Keeper resistor
STIN	IN with Pull-down resistor	IN with Keeper resistor
STOUT	OUT	OUT – High Level
RST/PD/	IN with Pull-up resistor	IN driven Low
X1 – X2	Oscillator	Power-down
XDIV	IN	IN with Keeper resistor
TEST	IN with Pull-down resistor	IN with Pull-down resistor

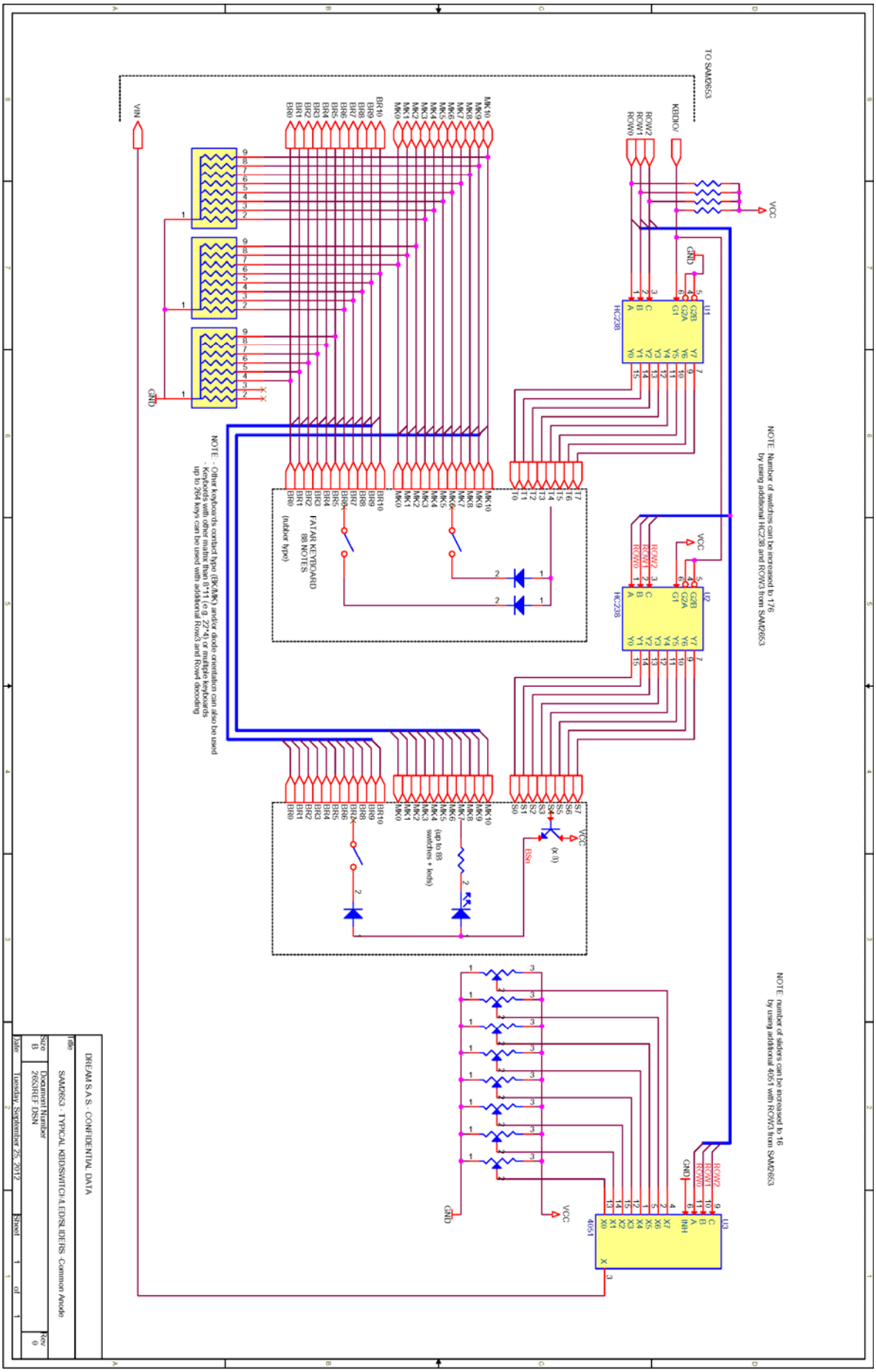
Note:

- Keeper resistor can be pull-up or to pull-down resistor. This will depend on logic state at the pin where it is connected when switching to Power-down mode.
    - If logic state is ‘Low’ when entering Power-down mode, keeper resistor will be pull-down
    - If logic state is ‘High’ when entering Power-down mode, keeper resistor will be pull-up
- In a designs where it is planned to use the Power-down mode, external pull up or pull down resistor should be added on each pin that have the “IN (floating)” status and that is not externally driven in Power-down mode. To avoid consumption in Normal mode these resistors can have high value like 1MOhm.

9- RECOMMENDED CRYSTAL COMPENSATION



10- TYPICAL KEVBOARD, SWITCHES, LEDS, SLIDERS CONNECTION



11- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VD33 distribution, decoupling

All GND, AGND, VD33, VA33 pins should be connected. A GND plane is strongly recommended below the SAM2653. The board GND + VD33 planes could be in grid form to minimize EMI.

Recommended decoupling is 4.7 or 10µF close to OUTVC12 pin. VD33 requires 0.1uF at each corner of the IC with an additional 10µFT capacitor should be placed close to the crystal.

- Crystal

The paths between the crystal, the crystal compensation capacitors and the SAM2653 should be short and shielded. The ground return from the compensation capacitors should be the GND plane from SAM2653.

- Busses

Parallel layout from DB0-DB7 and WA0-WA24/WD0-WD15 should be avoided. The DB0-DB7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA24/WD0-WD15 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the DB0-DB7 bus.

A ground plane should be implemented below the WA0-WA24/WD0-WD15 bus, which connects both to the ROM/Flash grounds and to the SAM2653.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

12- PRODUCT DEVELOPPMENT AND DEBUGGING

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (XP, Vista, Win7). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program external Flash, serial Flash, EEPROM on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available such as:

- GM Synth with reverb and chorus
- MIDI functions
- File access to SD Card

Dream engineers are available to study customer specific applications.

dream

SAM2653

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Website

http://www.dream.fr

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