SAM5504B

AUDIO & MUSIC MULTI-DSP PROCESSOR

Key features

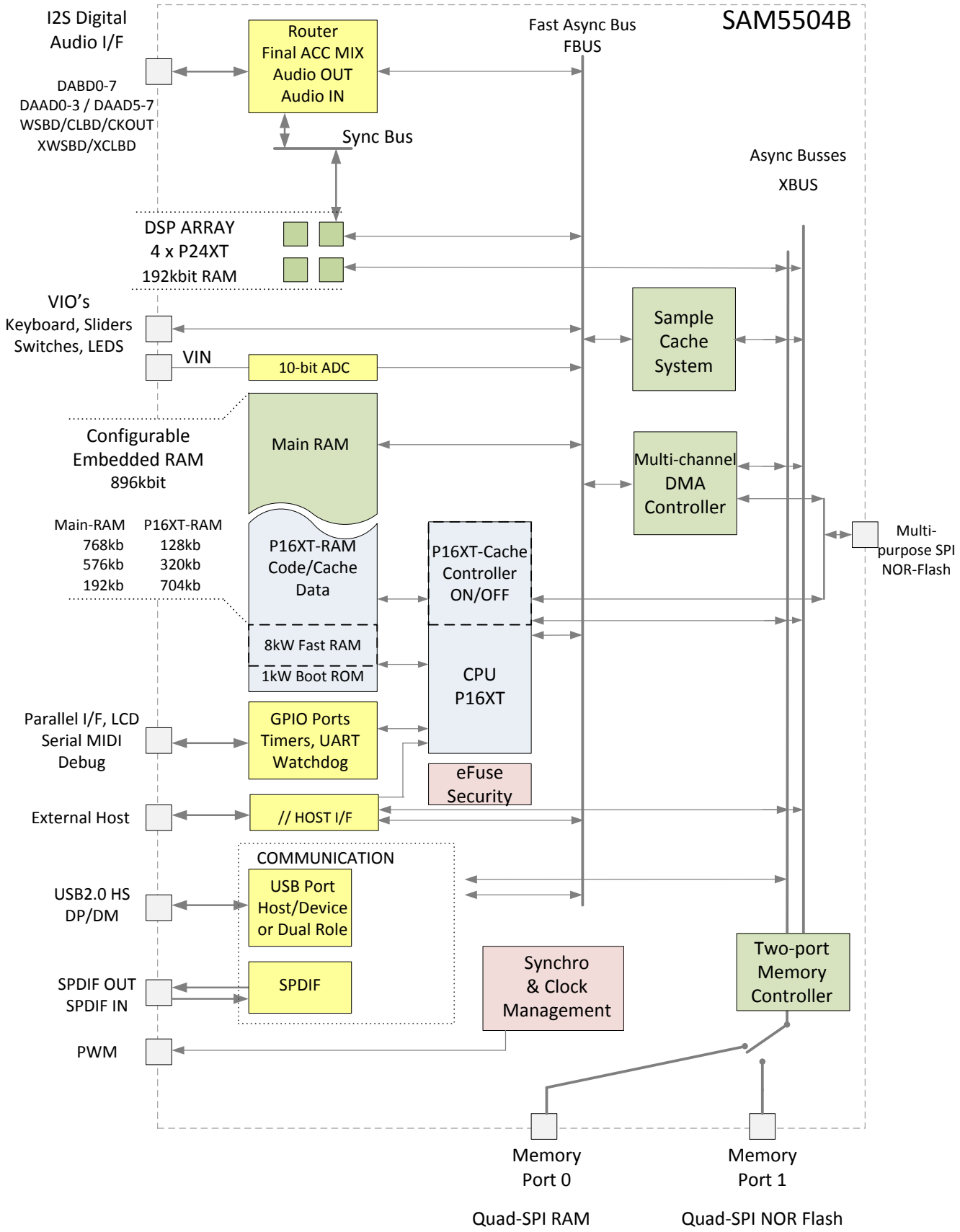
- **Dream DSP Array of 4 new 24bit/56bit DSP cores** (P24XT) supporting 56bit MAC operations (200M MAC/sec), vector processing, double precision instructions and offering a rich set of hardware accelerated macro-instructions (including 48x48bit multiply or double precision bi-quad filter)
- New highly **speed optimized 16bit CPU** (P16XT) running at 200MHz, with optimized instruction set for C compiler, interrupts, new fast 32-bit instructions, 512Kword max. program code size
- Built-in 1kbit eFuse for configuration and security (program code and sound bank protection)
- Built-in configurable fast **Data/Effect RAM up to 32Kx24** (or 48Kx16), + 8Kx24 DSP RAM
- Built-in configurable fast Program Code/Cache RAM, on-the-fly code decryption
- Multi-channel DMA for fast data transfers to external memories, supports circular buffers and transparent 24- to 16-bit transformation
- External memories: 2 flexible serial configurations (Quad-SPI-NOR, Quad-SRAM)
- On-the-fly wave sample decryption (AES encryption format with high security)
- 8-bit parallel slave Port capability for external Host control
- Multi-purpose SPI interface (single, mode 0) for Serial Flash, SD-Card, Graphic Display…
- 2 Serial MIDI IN/OUT (UART) interfaces
- **USB 2.0 High Speed** port (HOST, DEVICE) for USB-Disk (flash drive) or AudioClass compliant Audio/MIDI interface function, and other USB functions
- Up to **192kHz S/PDIF** interface (IEC60958) with clock recovery (concurrent IN/OUT)
- On-die synchronization PWM mechanism controlling external VCXO for audio streaming from external sources
- Up to 14 Audio channels IN / 14 Audio channels OUT, most Audio IN can be used in clock slave mode
- Direct connection to velocity keyboards (various types), LEDs, switches, sliders/potentiometers/ modulation wheels, SPI LCD or SPI Graphic Display and others
- Watchdog, Timers, Power reduction modes, unused primary interfaces can be used as GPIOs
- 64-pin LQFP package

Typical applications

- Low cost Keyboards, USB/MIDI Controller Keyboards…
- Effect devices, Speaker processing, USB Audio Interfaces…

1. SAM5504B Internal Architecture

1.1. Block Diagram



1.2. Overview

Based on a multi-layer architecture, the new family of DREAM's Audio & Music processors (SAM5000) is built around a new highly speed optimized 16-bit CPU (P16XT) and a configurable array of hardware accelerated 24-bit DSP cores (P24XT).

A Sample Cache System dedicated to sound synthesis allows SAM5000 processors to reach high levels of polyphony whatever the memory type used for sound bank storage. Moreover, this solution allows on-the-fly decryption of waves protected with strong AES(*) encryption.

The processing of delay lines in external memory is hugely facilitated with the integration of a multi-channel DMA controller. This controller performs fast memory-to-memory data transfers with some key features: burst modes and circular buffer structures are supported and data are automatically re-formatted (24-bit↔16-bit) when transfers are done from internal to external memories. Transfers can be done in parallel on several channels without requiring any assistance of the CPU or DSP cores.

The SAM5504B is part of the new generation of DREAM's audio & music processors and automatically inherits all above features. With an array of 4 P24XT DSP cores, the SAM5504B is delivered in a cost-efficient 64-pin QFP package. It is intended to low-cost keyboard, effect and professional audio applications.

In addition to a large variety of communication interfaces (USB 2.0 HS port, S/PDIF IN/OUT…), the SAM5504B has two memory ports supporting serial, memory types. Two different memory configurations can be defined with pull-resistor externally connected to dedicated pin. Memory configuration is read by boot program at power-up from dedicated pin or fuse bits.

The SAM5504B includes a 24-bit Audio Router and supports up to 14 Audio Channels IN & 14 Audio Channels OUT. Depending on primary functions in use, digital audio signals can be accessed via primary or secondary IO pads. Most of the IO pads that are not used for primary functions remain available for secondary functions or for firmware programmable IO functions (Versatile IO's or GPIO's).

The SAM5504B can handle up to 64 switches (organized in matrix form) and 64 LEDs (in a time multiplexed way) through versatile firmware programmable IO pads. Keyboard and switches scanning tasks can be fully customized in one dedicated P24XT, making the SAM5504B directly compatible with most of velocity keyboards. Similarly, LCD or graphic displays can be directly connected to programmable IO's and controlled by the P16XT.
A built-in ADC allows connecting continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc.

A built-in 1kbit eFuse provides a plenty of irreversible one-time-programmable bits for the storage of configuration parameters, decryption keys and other security purposes. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5504B.

(*) AES is the worldwide most used symmetric-key algorithm.

1.3. DSP Array – 4 * P24XT

The SAM5504B is built around an Array of 4 new 24-bit DSP cores (P24XT).

Similarly to previous generation, each P24XT DSP core includes a 2k x 24 RAM and a 2k x 24 ROM. The RAM contains both data and DSP instructions, while the ROM contains typical coefficients such as FFT cosines and windowing and micro-code for hardware accelerated micro-instructions.

The P24 sends and receives audio samples through the Sync Bus at the frame rate (typically, 48kHz frame period = 2048 cycles at 98.8 MHz). For the transfer of all other data, the P24XT is able to communicate in an asynchronous way through Async Busses. P24XT memories can be accessed through the Async Bus by others.

A lot of operations can be performed with much more precision with new P24XT core.
For single-precision operations:

- Programmable 24-bit fixed format: 1.0.23, 1.2.21, 1.8.15 or 1.15.8
- 56-bit MAC unit with 24-bit x 24-bit multiplication + 8 guard bits to prevent overflow issues

For double-precision operations:

- Programmable 48-bit fixed format: 1.0.47, 1.2.45, 1.8.39 or 1.15.32
- Large set of 48-bit Double Precision (DP) operations

The P24XT DSP core also offers hugely improved performances with a new and rich set of hardware accelerated macro-instructions:

  - ADD, MUL, MAC operations on vectors can be performed with only one macro-instruction, address pointers being self-incremented
  - ring buffer structures are supported in several vector instructions
  - several arithmetic operations are available: SIN, COS, DIV, LN, EXP, …
  - Operations on complex values in single and double precision
  - Polynomial calculation in single and double precision
  - Optimized filtering instructions: 1^{st} & 2^{nd} order filters, programmable number of taps, single or double precision

Based on polynomial interpolation, up to 27 sounds (at typical 48kHz frame clock) with high quality filtering can be synthesized within one P24XT, and up to 50M of 56-bit MAC operations can be performed per second.

1.4. Sync Bus

The Sync Bus transfers audio samples on a frame basis, typical frame rates being 44.1, 48, 96 & 192 kHz. Each frame is divided into 32 time slots. Each slot is divided into 8 bus cycles. Each P24XT is assigned a hardwired time slot (16 to 31), during which it may provide 24-bit data to the bus (up to 8 data samples). Each P24 can read data on the bus at any time, allowing inter-P24 communication at the current sampling rate. Slots 0 to 15 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

1.5. Async Busses

As shown in the general block diagram, several 24-bit Async Busses can be accessed by most of masters (P16XT, P24XT, DMA controller…) in a parallel way. Two busses XBUS0 & XBUS1 give access to external memories.

1.6. Enhanced 16-bit CPU – P16XT

The SAM5504B operates under the control of a new highly speed optimized 16-bit CPU (P16XT).

The key features of the P16XT are the following:

- Typ. operating frequency = 196.6 MHz
- New instructions including 32 bit data handling and 32x32 multiply
- Maximum executable program size = 512k words
- Backward compatibility with previous P16 products and optimized instruction set for C-compiler
- Interrupt handling: 3 interrupt signals, 32 sources with programmable Mask, Polarity & Triggering mode

A tightly coupled code/cache memory allows the P16XT to fetch code lines with reduced latency when needed. This memory can be either used as code memory when the whole firmware can be stored in internal memory or as cache memory (n-Way Set Associative Cache System) in other cases. The internal code/cache memory is loaded during the boot sequence (at power-up) by P16XT ROM boot program.

By default, the code/cache memory has a size of 256kbits (16k*16). Depending on performance requirements, the distribution of internal memory between code/cache and data/effect partitions can be modified as explained in the next paragraph.

The P16XT ROM holds the boot program as well as a debugger which uses a dedicated asynchronous serial line.

1.7. On-chip memory

Besides distributed memory in P24XT DSP cores (4 * 2Kx24-bit RAM for a total of 192kbits) and in communication controllers, the SAM5504B offers 896kbits of on-chip memory. One part of this memory (P16XT-RAM) is reserved for direct access by the P16XT (tightly coupled code/cache memory). The second part of this memory (MAIN-RAM) is used as data memory and can be accessed by any master through the asynchronous bus.

The memory partitioning is configurable by firmware. The memory space is divided into 4 banks:

- Bank 0 has a size of 128kbits and is accessed by P16XT only.
- Bank 1 has a size of 192kbits and can be either used as code/cache memory for P16XT or as main data memory
- Bank 2 has a size of 384kbits and can be either used as code/cache memory for P16XT or as main data memory
- Bank 3 has a size of 192kbits and is always used as main data ram

		RAMCFG='00'		RAMCFG='01'		RAMCFG='10'	
		P16XT RAM	Main RAM	P16XT RAM	Main RAM	P16XT RAM	Main RAM
Bank0	128 kbits	8kx16	-	8kx16	-	8kx16	-
Bank1	192 kbits	-	8kx24	12kx16	-	12kx16	-
Bank2	384 kbits	-	16kx24	-	16kx24	24kx16	-
Bank3	192 kbits	-	8kx24	-	8kx24	-	8kx24
Total		128kbits 8kx16	768kbits 32kx24	320kbits 20kx16	576kbits 24kx24	704kbits 44kx16	192kbits 8kx24

1.8. Multichannel DMA controller

The DMA controller is intended to perform high-speed memory-to-memory data transfers without using CPU resources: blocks can be copied from one source address to one destination address with a specified length, while both source and destination addresses are self-incremented. Taking advantage of the multi-layer architecture, this module can operate on several channels in parallel. Moreover, the DMA controller is able to automatically perform 24-bit to 16-bit transformation when data blocks are transferred from internal to external memories. For making the handling of delay lines easier, circular buffers are also supported.

Main features:

- The DMA controller has 4 channels
- programmable block length and source & destination addresses
- supports word and burst transfers
- supports ring buffers
- transparent 24-bit to 16-bit transformation

1.9. Sample Cache System

Thanks to its sample cache system, the SAM5504B can support up to 81 voices of polyphony with sound banks stored in Quad-SPI NOR.

1.10. Two-port memory controller

The two-port memory controller enables the SAM5504B to interface with different serial memory types:

Config	*Port0*	*Port1*	*KBD Interface*
1	-	QuadSPI-NOR	Yes
2	QuadSPI-SRAM	-	No

Memory configurations are defined with pull-resistor externally connected to dedicated pin and are read by boot program at power-up from dedicated pin or fuse bits.

Configuration 1 with low pin-count serial memory interfaces is dedicated to keyboard applications. Configuration 2 is dedicated to effect/audio processing/USB audio interface applications.

The two-port memory controller handles transfer requests initiated by masters like P16XT CPU, P24XT DSP cores, DMA controller, Sample cache system or other communication controllers through both XBUS asynchronous busses.

Control registers are accessed by the P16XT for defining configuration and optimizing frequency and latency parameters. Burst transfers are always initiated when possible.

1.11. Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 16 channels of audio in and 16 channels of audio out are provided (8 stereo in/out, I2S or MSB Left format). The stereo audio in channel may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

1.12. External Host Interface

The Host Parallel Interface is used for fast read/write transfers between an external host processor and the SAM5504B. E.g. it allows an external host to be a master for fast data transfer to SAM5504B connected memories (the handshake protocol for the fast data transfer is driven by the firmware).
This module is connected internally to asynchronous busses.

1.13. Versatile I/O's and GPIO's

Most of the IO pads, when not used for primary (or secondary) specific functions, remain available as firmware programmable IO pads. Programmable IO functions are divided into 2 categories:

- Versatile IO's when they can be controlled through asynchronous busses by either P16XT or P24XT cores for keyboard scanning, sliders, switches and LED's control.
- General Purpose IO's (GPIO's) when accessible by the P16XT only for functionalities like LCD Display control, …

1.14. High-speed USB 2.0 Port

USB Port allows the SAM5504B to connect it directly to

- an USB host (such as a PC) in device mode
- an USB device (such as a mass storage USB key) in host mode.

USB Port has PHY on-die.

1.15. S/PDIF – Sony/Philips Digital Interface

The S/PDIF audio module allows the SAM5504B to receive and transmit digital audio concurrently. The SAM5504B provides one single S/PDIF receiver with an input signal and one S/PDIF transmitter with another output signal.

For synchronization purposes, the audio clock can be recovered from the incoming audio stream.

1.16. Synchronization and clock management

Depending on the application, the SAM5504B supports 3 clock sources (OSC1, OSC2 & VCXO) for the generation of the reference clock (see table below) and 2 programmable PLL. With a crystal at 12.288MHz, the main PLL generates a clock at 393.2 MHz (32*12.288MHz). This high-frequency system clock is optionally divided through programmable dividers to generate several slower control clocks. Most of internal clocks can be stopped individually for flexible power optimization.

For audio streaming applications, the SAM5504B is able to behave as a slave. Synchronization to an external clock, extracted from input audio streaming for example, can be achieved by controlling an external VCXO with built-in PWM signal. Re-synchronized clock from VCXO can be used as 3rd clock source. In this case, the SAM5000 does use the clock from OSC1 (12MHz) during the start-up period.

Clock Mode	USB in use	Description	OSC1 (MHz)	OSC2 (MHz)	Audio Source Clock (MHz)	Typical (*) frame clock (kHz)
0	Yes	Single-Xtal 12MHz-USB	12	NU	12	46.875
1	No	Single-Xtal 12.288/11.2896MHz-Audio	12.288 11.2896	NU	12.288 11.2896	48 44.1
2	Yes	Two-Xtal 12MHz-USB + 12.288/11.2896MHz-Audio	12	12.288 11.2896	12.288 11.2896	48 44.1
3	Yes	Two-Xtal 12MHz-USB + VCXO	12	VCXO	VCXO	Ext. frame frequency

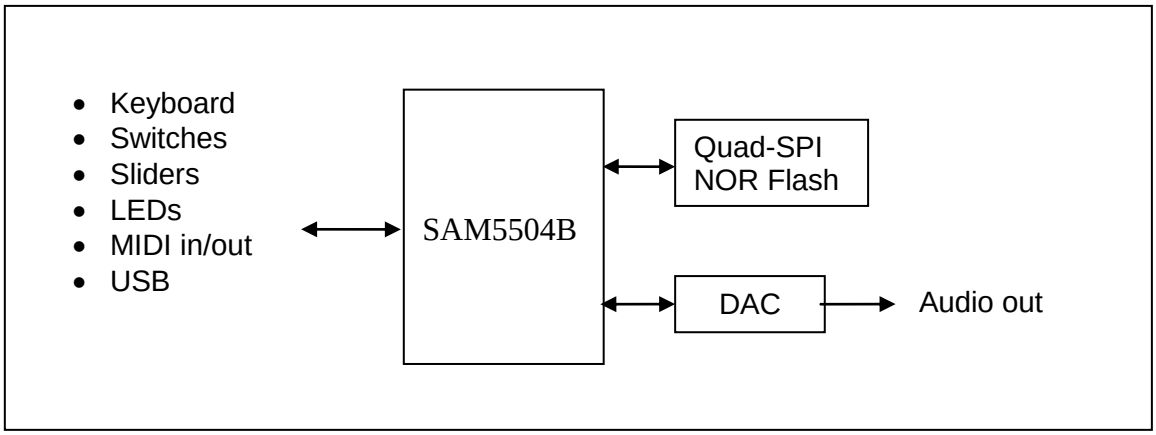
(*)SAM5000 supports 46.875kHz, 48/44.1KHz, 96/88.2KHz and 192/176.4KHz sampling rates

1.17. eFuse and security

A built-in 1kbit eFuse provides a plenty of irreversible One-Time-Programmable bits for the storage of configuration parameters, decryption keys and other security purpose data. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5504B.

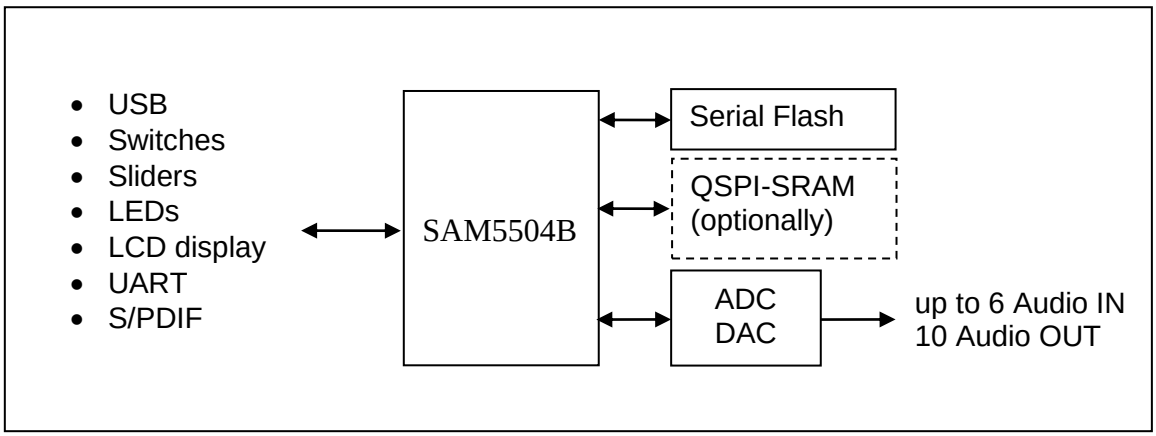
2. Typical application examples

2.1. **Low-Cost Keyboard with USB** (using Memory Configuration 1)



- 81 voice high quality sound synthesis (polynomial interpolation, new filter modes…) with sound banks in Quad-SPI-NOR
- Copy protected sound banks in cost saving memories (Quad-SPI-NOR, up to 128MByte)
- Effects processing (Reverb, Chorus, Equalizer) using in-build RAM memory
- Direct connection to keyboard, switches, LEDs
- 10-bit ADC for sliders and pedals (with embedded mux: 3 inputs available)
- USB-MIDI or USB-Disk

2.2. **Low-Cost Professional Audio Applications** (using Memory Configuration 2)



- USB 2.0 High Speed port e.g. for AudioClass 2.0 compliant USB Audio interface
- S/PDIF interface (IEC60958) with clock recovery (concurrent IN/OUT)
- Up to 6 Audio IN and 10 Audio OUT channels at up to 192KHz sampling rate / 24bit
- On-die synchronization PWM mechanism controlling external VCXO for audio streaming from external sources
- Vast library of ready to use high-class filters, dynamic processing, delays, effects of all kind…
- Typical applications: Speaker processing, USB Audio interfaces, Effect units etc.

3. SAM5504B capacity and I/O configuration

The SAM5504B can run a firmware from an external Quad-SPI NOR Flash or serial Flash/DataFlash/EEPROM memory, by using Cache mode or boot-load mechanism. A firmware can also be down-loaded from a Host CPU, and SAM5504B runs the firmware from local RAM. The SAM5504B can use its local RAM for effects processing (the embedded RAM is widely configurable for best choice between program and effects memory space), it can be extended by external low cost Quad-SPI RAM. The SAM5504B is the ideal choice for low cost keyboards, and also professional audio products like Mixer effect devices, Speaker processing, USB-Audio Interfaces etc., with low count of required external components and many configurable I/Os.

3.1. DSP considerations

The SAM5504B includes 4 x P24XT DSPs.
The table below lists the performance achievable by the P24:

Function	P24XTs required
81-voice Wavetable Synthesis @48kHz	3
stereo Reverb, Chorus, Equalizer and Keyboard Scanning @48kHz	1
56 double precision filters bands @48kHz	1
8 in / 8 out USB Audio Interface @48KHz	1

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pin-out to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host-controlled operation

There are 3 main ways of communication with a host processor:

- 8-bit parallel bi-directional Host interface
  signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial, 2x RX (MIDI_IN) and 2x TX (MIDI_OUT)
- Synchronous serial
  signals: SSDIN, SSCLK, SSYNC, SSINT/

3.2.2. Stand-alone operation

Possible stand-alone modes are:
- Firmware into external Flash connected on Quad-SPI NOR Flash bus (mem config 1)
- Firmware into external serial Flash connected on Multi-Purpose SPI bus (mem config 2)

4. SAM5504B PINOUT

4.1. Memory Config

The SAM5504B can be used in 2 different hardware configurations called Memory Config. This flexible architecture allows selecting the appropriate interfaces for each application.

Memory Config can be defined in two ways:
1. Sensed at start-up: Memory Config is defined by the level on MC0 pin sensed at start-up. MC0 is sensed on CKOUT.
2. Read from Efuse MC0 bit: Memory Config is preprogrammed in embedded eFuse. In this case MC0 pin will not be sensed.

4.1.1. Memory Config Table

MC0	Memory Config	Description
0	1	Quad NOR Flash + Versatile IOs (Keyboard applications)
1	2	Quad SRAM + Host Parallel + Multi-purpose SPI

4.2. Pin-out by pin

4.2.1. Memory Config 1: Quad NOR Flash + Versatile IOs (Keyboard application)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	17	QNR3	33	DABD1_VIN2	49	CKOUT
2	TEST	18	MK4	34	DAAD0_VIN1	50	ROW0
3	STIN	19	MK5	35	VIN0	51	ROW1
4	STOUT	20	MK6	36	**VA33**	52	ROW2
5	MIDI_IN1	21	MK7	37	**AGND**	53	QNRCK
6	MIDI_OUT1	22	**VD33**	38	SEL0	54	BR0
7	MK0	23	BR4	39	**VD33**	55	BR1
8	MK1	24	BR5	40	FSOURCE	56	**VD33O**
9	**VD33**	25	BR6	41	OSC1_X1	57	OSC2_X1
10	QNRCS/	26	BR7	42	OSC1_X2	58	OSC2_X2
11	MK2	27	**VD12**	43	**VD33U**	59	**GNDO**
12	MK3	28	BR2	44	USBDM	60	**GND**
13	**VD12**	29	BR3	45	USBDP	61	**VC12**
14	QNR0	30	DABD0	46	**GNDU**	62	**OUTVC12**
15	QNR1	31	CLBD	47	USBREF	63	**VD33R**
16	QNR2	32	WSBD	48	**GND**	64	**GNDR**

4.2.2. Memory Config 2: Quad SRAM + Host Parallel + Multi-purpose SPI

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	17	DABD2	33	D1_VIN2	49	CKOUT
2	TEST	18	QSR0	34	D0_VIN1	50	CS/
3	STIN	19	QSR1	35	VIN0	51	RD/
4	STOUT	20	QSR2	36	**VA33**	52	WR/
5	MIDI_IN1	21	QSR3	37	**AGND**	53	DAAD1
6	MIDI_OUT1	22	**VD33**	38	QSRCK	54	SPI0
7	SPICK	23	D4	39	**VD33**	55	SPI1
8	SPICS/	24	D5	40	FSOURCE	56	**VD33O**
9	**VD33**	25	D6	41	OSC1_X1	57	OSC2_X1
10	QSRCS/	26	D7	42	OSC1_X2	58	OSC2_X2
11	D2	27	**VD12**	43	**VD33U**	59	**GNDO**
12	D3	28	IRQ	44	USBDM	60	**GND**
13	**VD12**	29	A0	45	USBDP	61	**VC12**
14	DAAD0	30	DABD0	46	**GNDU**	62	**OUTVC12**
15	DAAD2	31	CLBD	47	USBREF	63	**VD33R**
16	DABD1	32	WSBD	48	**GND**	64	**GNDR**

4.3. Pin description

White cells describes Primary function of the pin
Grey cells describes Secondary function of the pin
Pink cells describes GPIO function of the pin
Green cells describes Alternate function of the pin
Yellow cells describes special function of the pin at start-up

PD indicates pin with built-in pull-down resistor. (PD) indicates that the pull-down can be disabled.
PU indicates pin with built-in pull-up resistor. (PU) indicates that the pull-down can be disabled.
5VT indicates a 5 volt tolerant Input or I/O pin.
DR4, DR8, DR12 indicates driving capability at VOL, VOH (see § 7.3.- D.C. Characteristics)
SR3: If GPIO is used as input, an external 330Ω (min) serial resistor is needed for safe ROM boot.

4.3.1. Power Supply Group

Pin name	Pin#	Type	Mem Cfg	Description
VD12	13,27	PWR	1,2	Power for the internal core, +1.2V nominal (1.2V ± 10 %). These pins must be connected to the output of the regulator OUTVC12 (pin 62). 100nF+10nF capacitors should be connected between each of these pins and a close ground plane. 10µF should be added on pin 13.
VC12	61	PWR	1,2	Power for the internal PLL, +1.2V nominal (1.2V ± 10 %). This pin must be connected to the output of the regulator OUTVC12 (pin 62). 10µF+100nF capacitors should be connected between this pin and a close ground plane.
VD33	9,22,39	PWR	1,2	+3.3V power for periphery. All these pins should be returned to nominal 3.3V. 100nF decoupling capacitors should be connected between these pins and ground plane
GND	48,60	PWR	1,2	Digital ground. These pins should be returned to ground plane
VD33O	56	PWR	1,2	+3.3V power for internal oscillator. A 100nF filtering capacitor should be connected between VD33O and GNDO.
GNDO	59	PWR	1,2	Digital ground for internal oscillator OSC2. This pin should be returned to the ground plane
VD33R	63	PWR	1,2	+3.3V power for internal 3.3V to 1.2 V regulator OSC2. A 10µF filtering capacitor should be connected between VD33R and GNDR.
GNDR	64	PWR	1,2	Digital ground for internal 3.3V to 1.2 V regulator. This pin should be returned to the ground plane
VD33U	43	PWR	1,2	+3.3V power for internal USB port. 10µF+100nF+10nF capacitors should be connected between VD33U and GNDU.
GNDU	46	PWR	1,2	Digital ground for internal USB port. This pin should be returned to a ground plane
VA33	36	PWR	1,2	Analog power for the ADC. Should be connected to a clean analog +3.3V nominal. 10µF+100nF capacitors should be connected between VA33 and AGND.
AGND	37	PWR	1,2	Analog ground for ADC. Should be returned to a clean analog ground plane.
OUTVC12	62	PWR	1,2	3.3V to 1.2 V regulators output. The built-in regulator gives 1.2V for internal use. VC12 and VD12 pins should also be connected to this pin. Decoupling capacitors 3.3µF+100nF or 4.7µF+100nF must be connected between OUTVC12 pin and GNDR

Pin name	Pin#	Type	Mem Cfg	Description
FSOURCE	40	PWR	1,2	Fuse Program source input. - Left open or grounded (recommended) for normal operation. - Connected to +3.3V/12mA(min) power supply for fuse programming. 10µF+100nF capacitors should be connected between FSOURCE and ground plane.

4.3.2. Test, Reset, Oscillators, USB, ADC, MIDI (UART), Debug

Pin name	Pin#	Type	Mem Cfg	Description
TEST	2	In PD	1,2	Test input. Should be grounded or left open.
RST/	1	In	1,2	Master reset and Power down. Schmitt trigger input. RST/ should be held low during at least 10ms after power is applied. On the rising edge of RST/ the chip enters its initialization routine.
OSC1_X1- OSC1_X2	41,42	-	1,2	Main Oscillator OSC1 - Dual crystal design: 12 MHz external crystal connection for USB embedded Ports. - Single crystal design: USB, System and audio clocks are derived fromOSC1. Crystal value can be: ° 12MHz if USB in use. ° 11.2896MHz or 12.288MHz if USB is not used - An external clock can be connected to OSC1_X1.
OSC2_X1- OSC2_X2	57,58	-	1,2	Secondary Oscillator OSC2 - Dual crystal design: System and audio clocks are derived from OSC2_X1-OSC2_X2. Crystal value can be 11.2896MHz or 12.288MHz. - Single crystal design: These pins should be left unconnected. - An external clock can be connected to OSC2_X1. (e.g., enslavement to external VCX0 driven by SAM5504B PWM generator)
USBDM	44	I/O	1,2	USB D- connection (analog) of USB Port
USBDP	45	I/O	1,2	USB D+ connection (analog) of USB Port
USBREF	47	In	1,2	A 12kΩ ± 1% resistor should be connected between this pin and GNDU. Unconnected if USB Port is not used.
VIN0	35	In	1,2	Analog input 0 of embedded ADC.
MIDI_IN1	5	In 5VT (PU)	1,2	Serial MIDI In (UART Rx)
MIDI_IN2	5	In 5VT (PU)	1,2	Additional Serial MIDI In (UART Rx)
P0.14	5	I/O 5VT (PU) DR4	1,2	General purpose I/O pin.
MIDI_OUT1	6	Out DR4	1,2	Serial MIDI Out (UART Tx)
P0.9	6	I/O DR4	1,2	General purpose I/O pin.
STIN	3	In PD	1,2	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. It should be grounded or left open for normal operation.
STOUT	4	Out DR4	1,2	Serial test output. 57.6 kbauds async output used for firmware debugging.
MIDI_IN2	4	In 5VT (PU)	1,2	Additional Serial MIDI In (UART Rx)
P0.15	4	I/O 5VT (PU) DR4	1,2	General purpose I/O pin.

4.3.3. Multi-purpose SPI as primary function

Pin name	Pin#	Type	Mem Cfg	Description
SPICK	7	Out DR8	2	Data clock for Multi-purpose SPI interface.
PWM_OUT	7	Out DR8	2	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.14	7	I/O 5VT DR8 SR3	2	General purpose I/O pin.
SPICS/	8	Out DR8	2	Chip select for Multi-purpose SPI interface.
P7.15	8	I/O 5VT (PU) DR8 SR3	2	General purpose I/O pin.
SPI0	54	Out DR12	2	SPI data 0. - Serial Output to SI peripheral Input (MOSI)
SPDIF_OI	54	I/O 5VT DR12	2	SPDIF Output or Input. Output by default.
P7.10	54	I/O.5VT DR12 SR3	2	General purpose I/O pin.
SPI1	55	In 5VT	2	SPI data 1. - Serial Input from SO peripheral Output (MISO)
SPDIF_IO	55	I/O 5VT DR12	2	SPDIF Input or Output. Input by default.
P7.11	55	I/O.5VT DR12	2	General purpose I/O pin.

4.3.4. Host Parallel Interface as primary function

Pin name	Pin#	Type	Mem Cfg	Description
D0-D1 D2-D7	34,33, 11,12, 23-26	I/O DR8 I/O 5VT DR12	2	Host parallel interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0 address input.
DAAD2	34	In	2	Stereo audio digital input 2, I2S or MSB format.
DABD4	33	Out DR8	2	Stereo audio digital output 4, I2S or MSB format.
DABD3	11	Out DR12	2	Stereo audio digital output 3, I2S or MSB format.
DABD2	12	Out DR12	2	Stereo audio digital output 2, I2S or MSB format.
XWSBD1	23	In 5VT	2	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD1	24	In 5VT	2	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD0	25	In 5VT	2	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
XCLBD0	26	In 5VT	2	External clock bit for digital audio inputs DAAD[7:0].
P0.0-P0.1 P0.2-P0.7	34,33, 11,12, 23-26	I/O DR8 I/O 5VT DR12	2	General purpose I/O pins. Can be individually programmed as input or output.
VIN1-VIN2	34,33	In	2	Analog input 1 and input 2 of embedded ADC.
IRQ	28	Out DR12	2	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	28	Out DR12	2	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8_IntA	28	I/O 5VT DR12	2	General purpose I/O pin. External Interrupt source IntA.
A0	29	In 5VT	2	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	29	In 5VT	2	Serial Slave Synchronous Interface clock input.
P0.10	29	I/O 5VT DR12	2	General purpose I/O pin.
CS/	50	In 5VT	2	Host parallel interface chip select, active low.
SSYNC	50	In 5VT	2	Serial Slave Synchronous Interface input sync signal.
P0.11	50	I/O 5VT DR8	2	General purpose I/O pin.
WR/	52	In 5VT	2	Host parallel interface write, active low. D7-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	52	In 5VT	2	Serial Slave Synchronous Interface input data.
P0.12	52	I/O 5VT DR8	2	General purpose I/O pin.
RD/	51	In 5VT	2	Host parallel interface read, active low. D7-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	51	Out 5VT	2	Additional Serial MIDI Out (UART Tx) **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	51	I/O 5VT DR8	2	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot.** **If used as input, should not be driven low by external device while ROM boot.**

4.3.5. Versatile IOs as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MK0-MK1	7,8,	I/O 5VT DR8	1	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: Second Kbd contact / switch status. When SEL0=1 then MK[0-7] holds the keyboard key-on or second contact status. When SEL0=0 then MK[0-7] gives the switch status from ROW[0-2].
MK2-MK7	11,12, 18-21	I/O 5VT DR12		
BR0-BR7	54,55, 28,29, 23-26	I/O 5VT DR12	1	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: First Kbd contact / Led data. When SEL0=1 then BR[0-7] holds the keyboard key-off or first contact status. When SEL0=0 then BR[0-7] holds the led data from ROW[0-2].
DAAD7	54	In 5VT	1	Stereo audio digital input 7, I2S or MSB format.
DABD7	55	Out DR12	1	Stereo audio digital output 7, I2S or MSB format.
DAAD6	28	In 5VT	1	Stereo audio digital input 6, I2S or MSB format.
DABD6	29	Out DR12	1	Stereo audio digital output 6, I2S or MSB format.
DABD3	23	Out DR12	1	Stereo audio digital output 3, I2S or MSB format.
DAAD2	24	In 5VT	1	Stereo audio digital input 2, I2S or MSB format.
DAAD1	25	In 5VT	1	Stereo audio digital input 1, I2S or MSB format.
ROW0-ROW2	50-52	I/O 5VT DR8	1	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: ROW signals select keyboard, switches/Leds row and external slider analog multiplexer (4051) channel. Height rows combined with 8 BR/MK columns allow to control 64 keys, 64 switches, 64 Leds and 8 sliders.
DAAD5	50	In 5VT	1	Stereo audio digital input 5, I2S or MSB format.
DABD4	51	Out DR8	1	Stereo audio digital output 4, I2S or MSB format.
DABD5	52	Out DR8	1	Stereo audio digital output 5, I2S or MSB format.
SEL0	38	I/O 5VT DR8	1	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: If SEL0=1, BR[0-7] & MK[0-7] hold keyboard contact input data. If SEL0=0 MK[0-7] holds switch status input, BR[0-7] holds led data output..
DAAD3	38	In 5VT	1	Stereo audio digital input 3, I2S or MSB format.

4.3.6. Quad SPI NOR Flash as primary function

Pin name	Pin#	Type	Mem Cfg	Description
QNRCK	53	Out DR4	1	Data clock for QSPI NOR Flash interface.
P7.9	53	I/O 5VT DR4 SR3	1	General purpose I/O pin.
QNRCS/	10	Out DR12	1	Chip select 0 for QSPI NOR Flash interface.
P1.14	10	I/O 5VT (PU) DR12 SR3	1	General purpose I/O pin..
QNR0	14	I/O 5VT DR12	1	QSPI NOR Flash data 0. - Serial Output to SI peripheral Input for Single bit data commands. - Serial IO0 for Quad operations.
P7.5	14	I/O 5VT DR12 SR3	1	General purpose I/O pin.
QNR1	15	I/O 5VT DR12	1	QSPI NOR Flash data 1. - Serial Input from SO peripheral Output for Single bit data commands. - Serial IO1 for Quad operations.
P7.6	15	I/O 5VT DR12 SR3	1	General purpose I/O pin.
QNR2-QNR3	16-17	I/O 5VT DR12	1	QSPI NOR Flash data 2-3. Serial IO2-IO3 for Quad operations
P7.7-P7.8	16-17	I/O 5VT DR12 SR3	1	General purpose I/O pin.

4.3.7. Quad SPI SRAM as primary function

Pin name	Pin#	Type	Mem Cfg	Description
QSRCK	38	Out DR8	2	Data clock for QSPI SRAM interface.
P7.4	38	I/O 5VT DR8	2	General purpose I/O pin.
QSRCS/	10	Out DR12	2	Chip select 0 for QSPI SRAM interface.
P1.13	10	I/O 5VT (PU) DR12	2	General purpose I/O pin.
QSR0	18	I/O 5VT DR12	2	QSPI SRAM data 0. - Serial Output to SI peripheral Input for Single bit data commands. - Serial IO0 for Quad operations.
P7.0	18	I/O 5VT DR12	2	General purpose I/O pin.
QSR1	19	I/O 5VT DR12	2	QSPI SRAM data 1. - Serial Input from SO peripheral Output for Single bit data commands. - Serial IO1 for Quad operations.
P7.1	19	I/O 5VT DR12	2	General purpose I/O pin.
QSR2-QSR3	20-21	I/O 5VT DR12	2	QSPI SRAM data 2-3. Serial IO2-IO3 for Quad operations
P7.2-P7.3	20-21	I/O 5VT DR12	2	General purpose I/O pin.

Note: This Quad SPI interface can also be used to connect a Quad SPI NOR Flash.

4.3.8. Digital Audio as primary function

Pin name	Pin#	Type	Mem Cfg	Description
CKOUT	49	Out DR4	1,2	Audio master clock for external DAC and ADC. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, 768xFs, Fs being the DAC and ADC sampling rate.
MC0	49	In	1,2	Memory Config 0. This pin is sensed at power up. MC0 setting allows boot ROM code to start the right Memory Config.
CLBD	31	Out DR4	1,2	Audio bit clock for DABD0-DABD7 and for DAAD0-DAAD3, DAAD5-DAAD7.
FS1	31	In	1,2	Freq. Sense 1, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq. on oscillator OSC1 as follow: 00->12MHz 01->9.6MHz, 10->11.2896MHz, 11->12.288MHz
WSBD	32	I/O DR4	1,2	Out by default: Audio left/right channel select for DABD0-DABD7 and for DAAD0-DAAD3, DAAD5-DAAD7. In: WSBD from external master audio device for full audio sync without external VCXO. Same Master clock is needed on SAM5504B and external master device.
FS0	32	In	1,2	Freq. Sense 0, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq on OSC1 (see FS1).
DAAD0	34	In (PD)	1	Stereo audio data input 0, I2S or MSB format.
SPDIF_IO	34	I/O (PD) DR8	1	SPDIF Input or Output. Input by default.
P2.0	34	I/O (PD) DR8	1	General purpose I/O pin.
VIN1	34	In	1	Analog input 1 of embedded ADC.
DAAD0	14	In 5VT (PD)	2	Stereo audio digital input 0, I2S or MSB format.
SPDIF_IO	14	I/O 5VT (PD) DR12	2	SPDIF Input or Output. Input by default.
P2.0	14	I/O 5VT (PD) DR12	2	General purpose I/O pin.
DAAD1	53	In 5VT (PD)	2	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	53	Out DR4	2	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	53	I/O 5VT (PD) DR4	2	General purpose I/O pin.
DAAD2	15	In 5VT (PD)	2	Stereo audio digital input 2, I2S or MSB format.
MIDI_OUT2	15	Out DR12	2	Additional Serial MIDI Out (UART Tx)
P2.2	15	I/O 5VT (PD) DR12	2	General purpose I/O pin.
DABD0	30	Out DR12	1,2	Stereo audio digital output 0, I2S or MSB format.
SPDIF_OI	30	I/O 5VT DR12	1,2	SPDIF Output or Input. Output by default.
P2.15	30	I/O 5VT DR12	1,2	General purpose I/O pin.
DABD1	33	Out DR8	1	Stereo audio digital output 1, I2S or MSB format..
P2.8	33	I/O (PU) DR8	1	General purpose I/O pin.
VIN2	33	In	1	Analog input 2 of embedded ADC.
DABD1	16	Out DR12	2	Stereo audio digital output 1, I2S or MSB format..
P2.8	16	I/O 5VT (PU) DR12	2	General purpose I/O pin.
DABD2	17	Out DR12	2	Stereo audio digital output 2, I2S or MSB format.
P2.9	17	I/O 5VT DR12	2	General purpose I/O pin.

4.4. Primary & Secondary functions quick view

4.4.1. Key table

Function Code	Function description	Available in…
1	Multi-purpose Single SPI interface	Mem. Config. 2
2	Host Parallel Interface (8-bit)	Mem. Config. 2
3	UART / MIDI interface	Mem. Config. 1,2
4	Debug interface	Mem. Config. 1,2
5	Serial Slave Synchronous interface	Mem. Config. 2
6	I2S Digital Audio Interface	Mem. Config. 1,2 (see Note1)
7	SPDIF Digital Audio Interface	Mem. Config. 1,2
8	Versatile IOs (VIO)	Mem. Config. 1
9	Quad SPI NOR Flash Controller on Memory Port 1	Mem. Config. 1
10	Quad SPI SRAM Controller on Memory Port 0	Mem. Config. 2
11	USB High Speed Host or Device	Mem. Config. 1,2

Note1: All Digital Audio Signals are not available for each Memory Configuration.

4.4.2. Functions per pin

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	TST				Config 1-6
	RST/				Config 1,2
	OSC2_X1-OSC2_X2				Config 1,2
	VIN				Config 1,2
3	MIDI_OUT1 (UART Tx)			P0,9	Config 1,2
3	MIDI_IN1 (UART Rx)	3	MIDI_IN2	P0.14	Config 1,2
4	STIN				Config 1,2
4	STOUT	3	MIDI_IN2	P0.15	Config 1,2
	Multi-purpose Quad SPI				
1	SPICK		PWM_OUT	P7.14	Config 2
1	SPICS/			P7.15	Config 2
1	SPI0 (MOSI)	7	SPDIF_OI	P7.10	Config 2
1	SPI1 (MISO)	7	SPDIF_IO	P7.11	Config 2
	Host Parallel Interface				
2	D0	6	DAAD2	P0.0	Config 2
2	D1	6	DABD4	P0.1	Config 2
2	D2	6	DABD3	P0.2	Config 2
2	D3	6	DABD2	P0.3	Config 2
2	D4	6	XWSBD1	P0.4	Config 2
2	D5	6	XCLBD1	P0.5	Config 2
2	D6	6	XWSBD0	P0.6	Config 2
2	D7	6	XCLBD0	P0.7	Config 2
2	IRQ	5	SSINT/	P0.8/INTA	Config 2
2	A0	5	SSCLK	P0.10	Config 2
2	CS/	5	SSYNC	P0.11	Config 2
2	WR/	5	SSDIN	P0.12	Config 2
2	RD/	3	MIDI_OUT2	P0.13	Config 2
	Versatile IOs				
8	MK0-MK7				Config 1
8	BR0	6	DAAD7		Config 1
8	BR1	6	DABD7		Config 1
8	BR2	6	DAAD6		Config 1
8	BR3	6	DABD6		Config 1
8	BR4	6	DABD3		Config 1
8	BR5	6	DAAD2		Config 1
8	BR6	6	DAAD1		Config 1
8	BR7				Config 1
8	ROW0	6	DAAD5		Config 1
8	ROW1	6	DABD4		Config 1
8	ROW2	6	DABD5		Config 1
8	SEL0	6	DAAD3		Config 1

(To be continued)

(Continued)

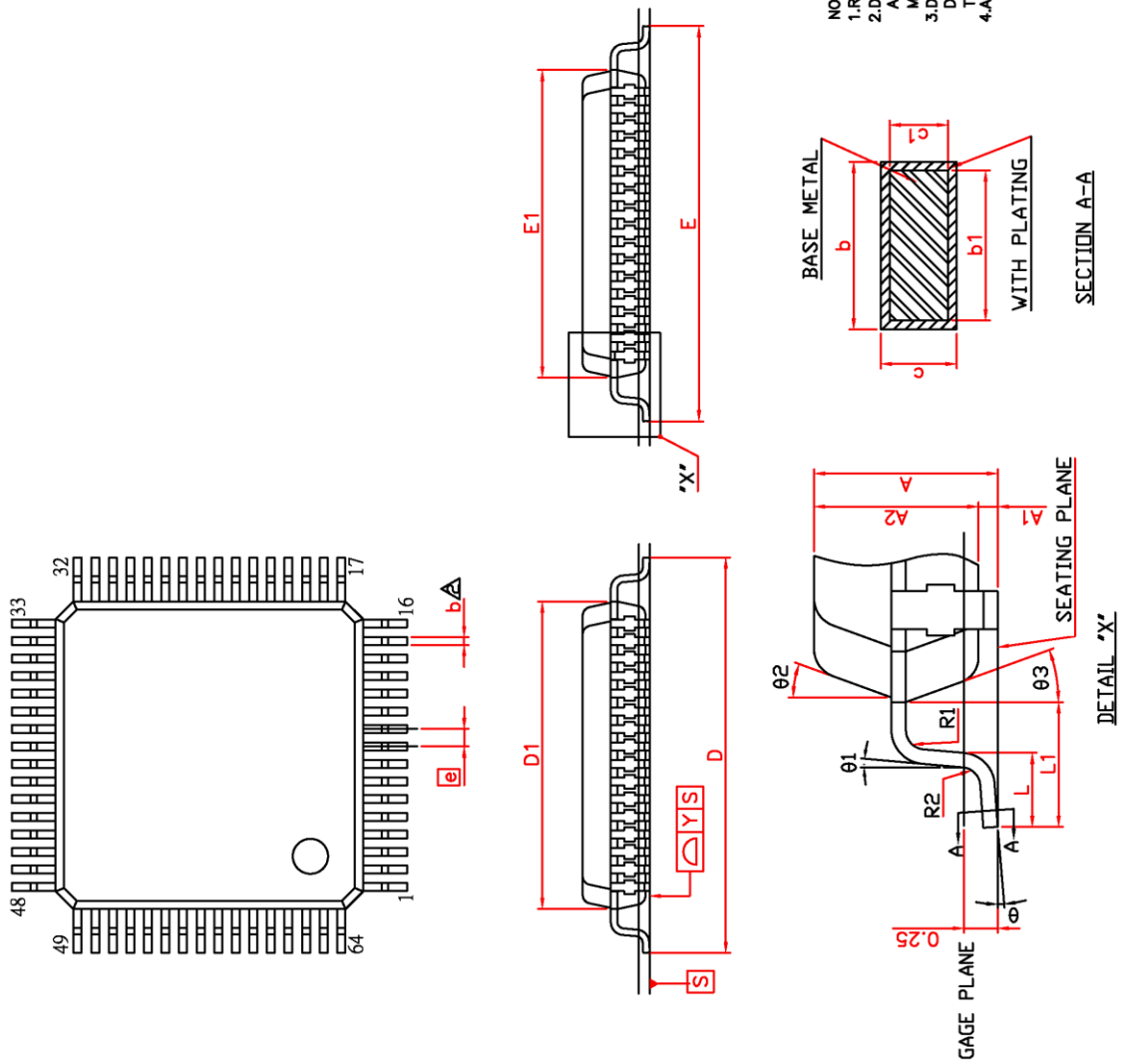
Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	Digital Audio				
6	CKOUT				Config 1,2
6	WSBD				Config 1,2
6	CLBD				Config 1,2
6	DAAD0	7	SPDIF_IO	P2.0	Config 1,2
6	DAAD1		PWM_OUT	P2.1	Config 2
6	DAAD2	3	MIDI_OUT2	P2.2	Config 2
6	DABD0	7	SPDIF_OI	P2,15	Config 1,2
6	DABD1			P2.8	Config 1,2
6	DABD2			P2.9	Config 2
	Quad SPI NOR Flash				
9	QNRCK			P7.9	Config 1
9	QNRCS0/			P1.14	Config 1
9	QNR0-QNR3			P7.5-P7.8	Config 1
	Quad SPI SRAM				
10	QSRCK			P7.4	Config 2
10	QSRCS/			P1.13	Config 2
10	QSR0-QSR3			P7.0-P7.3	Config 2
	USB Port				
11	OSC1_X1-OSC1_X2				Config 1,2
11	USBDP-USBDM				Config 1,2
11	USBREF				Config 1,2

5. Mechanical dimensions

64-pin LQFP Package

SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.40 BSC			15.8 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE C)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.



ZI 21140 Semur-en-Auxois FRANCE	**TITLE:** **LQFP64 (7 x 7 x 1.4mm) Package Outline** - Foot Print : 2 mm	**Package designation** LQFP64	**REV.** **2**

6. Marking

LQFP64

7. Electrical Characteristics

7.1. Absolute Maximum Ratings(*)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on 5 volt tolerant pin (5VT)	-	-0.3	-	5.5	V
Voltage on standard pin	-	-0.3	-	VD33+0.3	V
Supply voltage	VD12	-0.3	-	1.32	V
	VC12	-0.3	-	1.32	V
	VD33	-0.3	-	3.63	V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core supply voltage	VD12	1.1	1.2	1.3	V
PLL supply voltage	VC12	1.1	1.2	1.3	V
Periphery supply voltage	VD33	3	3.3	3.6	V
ADC supply voltage	VA33	3	3.3	3.6	V
Operating ambient temperature	tA	0	-	70	°C
Pull Resistor on MC[2:0] and FS[1:0] pins	RCFG	4.7k	10k	22k	Ohm

7.3. D.C. Characteristics (TA=25°C, VD12=VC12=1.2V±10%, VD33=3.3V±10%)

7.3.1. Standard LVTTL pads

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage on **5VT** pins	VIH	2	-	-	V
High level input voltage on non **5VT** pins	VIH	2	-	-	V
Low level output voltage (IOL =4 ~ 12mA)	VOL	-	-	0.4	V
High level output voltage (IOH =4 ~ 12mA	VOH	2.4	-	-	V
Schmitt-trigger negative-to-threshold voltage (RST/ pin)	VTN	0.8	1.1	-	V
Schmitt-trigger positive-to-threshold voltage (RST/ pin)	VTP	-	1.6	2	V
Driving capability at VOL, VOH for **DR4** pins	IOHL	-	-	4	mA
Driving capability at VOL, VOH for **DR8** pins	IOHL	-		8	mA
Driving capability at VOL, VOH for **DR12** pins	IOHL	-		12	mA
Input leakage current	IIN	-	±1	±10	µA
Built-in pull-up / pull-down resistor	RUD	40	75	190	kOhm

7.3.2. Analog I/O pins (USBDP, USBDM)

Parameter	Symbol	Min	Typ	Max	Unit
High-speed differential input sensitivity VI(USBDP)-VI(USBDM)	VHSDIF	300	-	-	mV
Voltage range input of the high-speed data signaling in the common mode	VHSCM	-50	-	500	mV
High-speed idle-level output voltage (Differential)	VHSOI	-10	-	10	mV
High-speed low-level output voltage (Differential)	VHSOL	-10	-	10	mV
High-speed high-level output voltage (Differential)	VHSOH	-360	-	400	mV
Driver output impedance.	RDRV	40.5	45	49.5	Ohm

7.3.3. General Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
OUTVC12 output voltage	VD12	1.14	1.2	1.26	V
VD33 power supply current in warm power down (PLL stopped, Sys clk = 12.288MHz crystal, all P24 stopped)	ID33	-	6	-	mA
VD33 power supply current in reset mode (RST/=0)	ID33	-	0.1	-	mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped)	ID33		34		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 running)	ID33		76		mA
VA33 power supply current (ADC running @ 11MHz)	IA33	-	3.2	-	mA
VA33 power supply current in reset mode	IA33	-	-	<1	µA
USB Full Speed current	ID33U	-	16	-	mA
USB High Speed current	ID33U	-	29	-	mA

7.4. ADC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Analog bottom internal reference voltage	VRefN	-	100	150	mV
Analog top internal reference voltage	VRefP	VA33-175	VA33-125	-	mV
Resolution	RES	-	10	-	bit
Integral non-linearity error	INL	-2	±1	+2	LSB
Clock frequency	ADCCK	1	-	11	MHz
Sampling Rate	ADCSR	-	-	1	MSps

8. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by a variable multiplication factor (typ. x16) to generate the internal chip system clock (“SysClk”, typ. 196.6MHz @ 12.288MHz quartz).
“spck” is the period of the internal clock. Typical value with Xtal = 12.288 MHz is spck = 5.1 ns.

8.1. Multi-purpose SPI interface

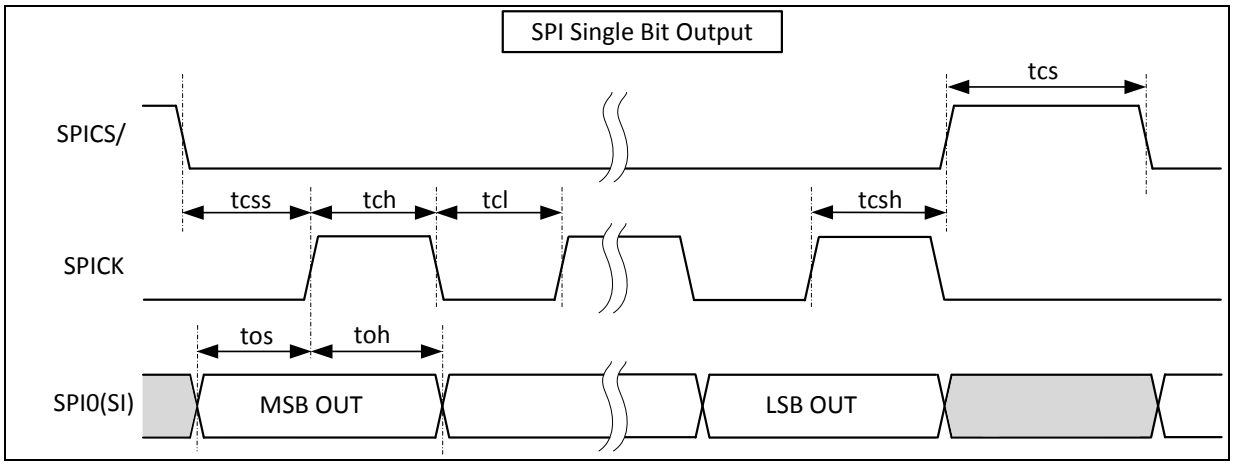
This is a master synchronous serial interface, operating in Single SPI mode 0.
SPI mode is driven by a powerful SPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

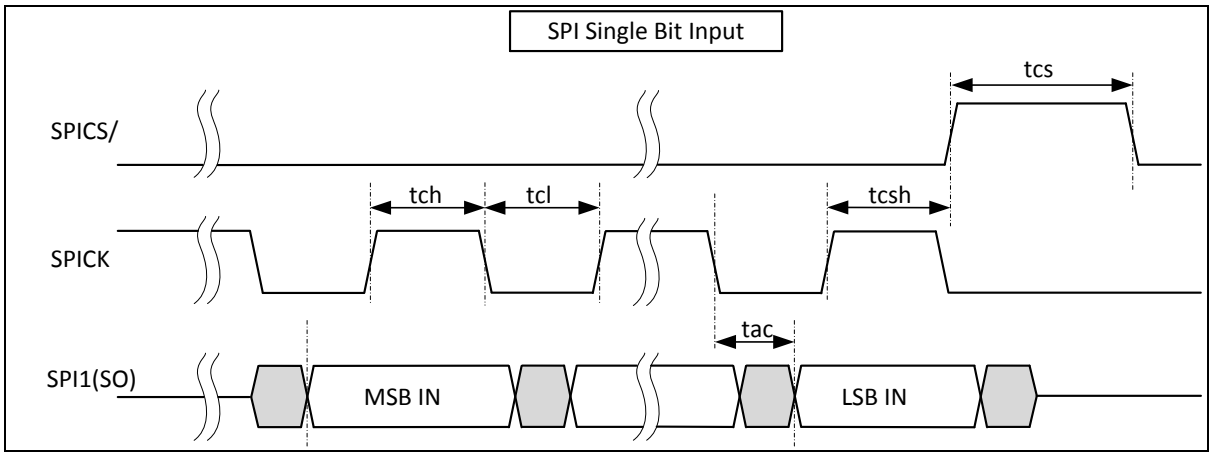
Single SPI mode can be driven by the SPI controller, but also by a Simple SPI interface through two IO registers.

Pins used:

SPICK: Clock output
SPICS/: Chip select
SPI0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
SPI1: Serial Input to be connected to SO output of SPI peripheral (MISO)

8.1.1. Timing





The SPI controller works on SysClk (usually 196.608MHz with Xtal = 12.288MHz).
SPICK frequency is SysClk/Nq. Nq can be programmed between 2 and 4096.

Parameter	Symbol	Min	Typ	Max	Unit
SPICK Frequency	fspick	SysClk/4096	-	SysClk/2	Hz
Clock High Time (even Nq)	tch	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock High Time (odd Nq)	tch	0.5*spck*(Nq-1)-0.5		0.5*spck*(Nq-1)+0.5	ns
Clock Low Time (even Nq)	tcl	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock Low Time (odd Nq)	tcl	0.5*spck*(Nq+1)-0.5		0.5*spck*(Nq+1)+0.5	ns
CS/ High Time	tcs	spck*Nq-1.5			ns
CS/ Active Setup Time (relative to SPICK)	tcss	spck*Nq-1.5			ns
CS/ Active Hold Time (relative to SPICK)	tcsh	spck*Nq-2.5			ns
Access Time from falling clock edge	tac	0.5		Spck*Nq-2.5	ns

8.2. Quad SPI NOR Flash interface

This is a master synchronous serial interface Quad SPI mode0, usually dedicated to audio samples import from Quad SPI NOR Flash.
Standard operating modes is Quad SPI. However, Single SPI mode is also allowed.

Quad SPI mode is driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

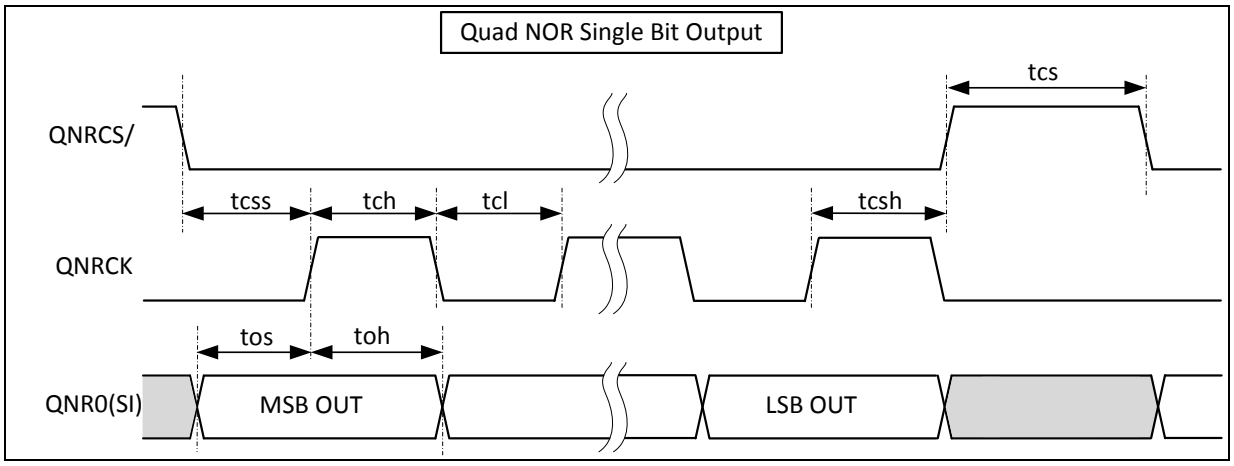
Pins used in Single SPI:

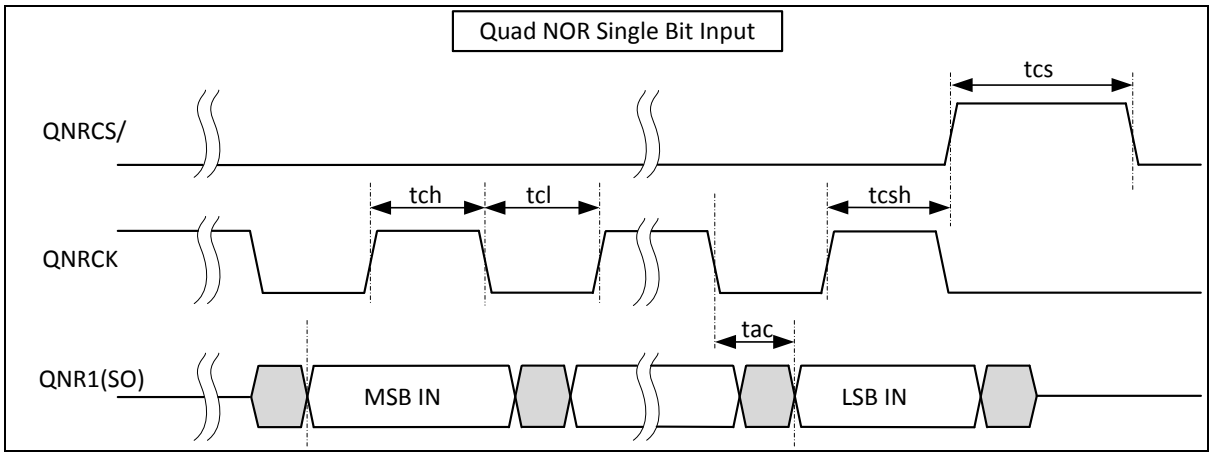
QNRCK: Clock output
QNRCS0/: Chip select
QNR0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
QNR1: Serial Input to be connected to SO output of SPI peripheral (MISO)

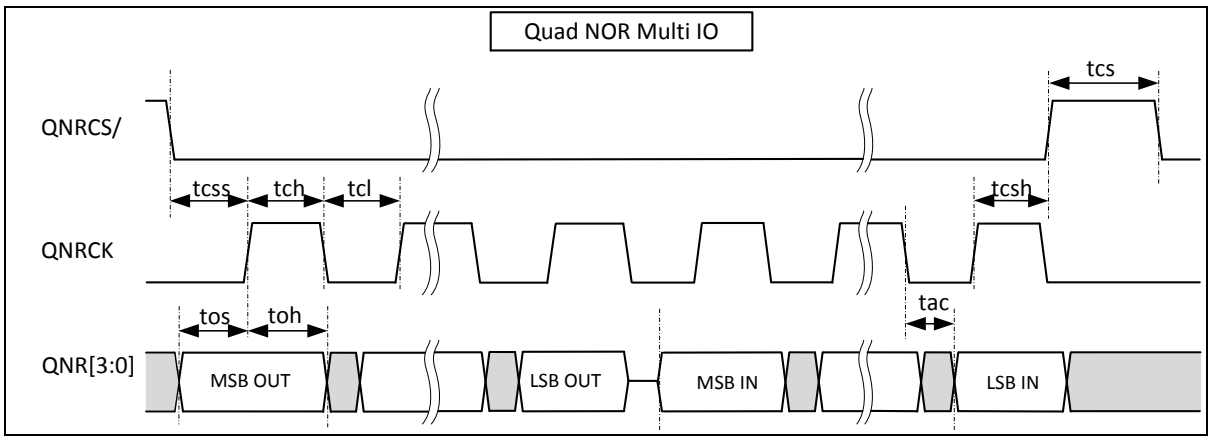
Pins used in Quad SPI:

QNRCK: Clock output
QNRCS0/: Chip select for
QNR0: Serial IO0 for Quad commands and data
QNR1: Serial IO1 for Quad commands and data
QNR2: Serial IO2 for Quad commands and data
QNR3: Serial IO3 for Quad commands and data

8.2.1. Timing







The QSPI controller works on SysClk (usually 196.608MHz with Xtal = 12.288MHz).
SPICK frequency is SysClk/Nq. Nq can be programmed between 2 and 4096.

Parameter	Symbol	Min	Typ	Max	Unit
SPICK Frequency	fspick	SysClk/4096	-	SysClk/2	Hz
Clock High Time (even Nq)	tch	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock High Time (odd Nq)	tch	0.5*spck*(Nq-1)-0.5		0.5*spck*(Nq-1)+0.5	ns
Clock Low Time (even Nq)	tcl	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock Low Time (odd Nq)	tcl	0.5*spck*(Nq+1)-0.5		0.5*spck*(Nq+1)+0.5	ns
CS/ High Time	tcs	spck*Nq-1.5			ns
CS/ Active Setup Time (relative to SPICK)	tcss	spck*Nq-1.5			ns
CS/ Active Hold Time (relative to SPICK)	tcsh	spck*Nq-2.5			ns
IO Out Setup Time(even Nq)	tos	0.5*spck*Nq-1.5			ns
IO Out Setup Time(odd Nq)	tos	0.5*spck*(Nq+1)-1.5			ns
IO Out Hold Time(even Nq)	toh	0.5*spck*Nq-2.5			ns
IO Out Hold Time(odd Nq)	toh	0.5*spck*(Nq-1)-2.5			ns
Access Time from falling clock edge	tac	0.5		Spck*Nq-2.5	ns

8.3. Quad SPI SRAM interface

This is a master synchronous serial interface Quad-SPI mode0, usually dedicated to effect processing in external Quad-SPI SRAM. However, this interface can also be used to connect an Quad-SPI NOR Flash.
Standard operating modes is Quad SPI but Single SPI mode is also allowed.

Quad SPI mode is driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

Pins used in Single-SPI:

QSRCK: Clock output
QSRCS/: Chip select
QSR0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
QSR1: Serial Input to be connected to SO output of SPI peripheral (MISO)

Pins used in Quad-SPI:

QSRCK: Clock output
QSRCS/: Chip select
QSR0: Serial IO0 for Quad commands and data
QSR1: Serial IO1 for Quad commands and data
QSR2: Serial IO2 for Quad commands and data
QSR3: Serial IO3 for Quad commands and data

8.3.1. Timing

Timing characteristics of the Quad-SPI SRAM interface are identical to timing characteristics of the Quad-SPI NOR Flash interface. See §7.2.1.

8.4. Host Parallel Interface

This interface is used to connect the SAM5504B to an external host processor for control and fast data transfer.

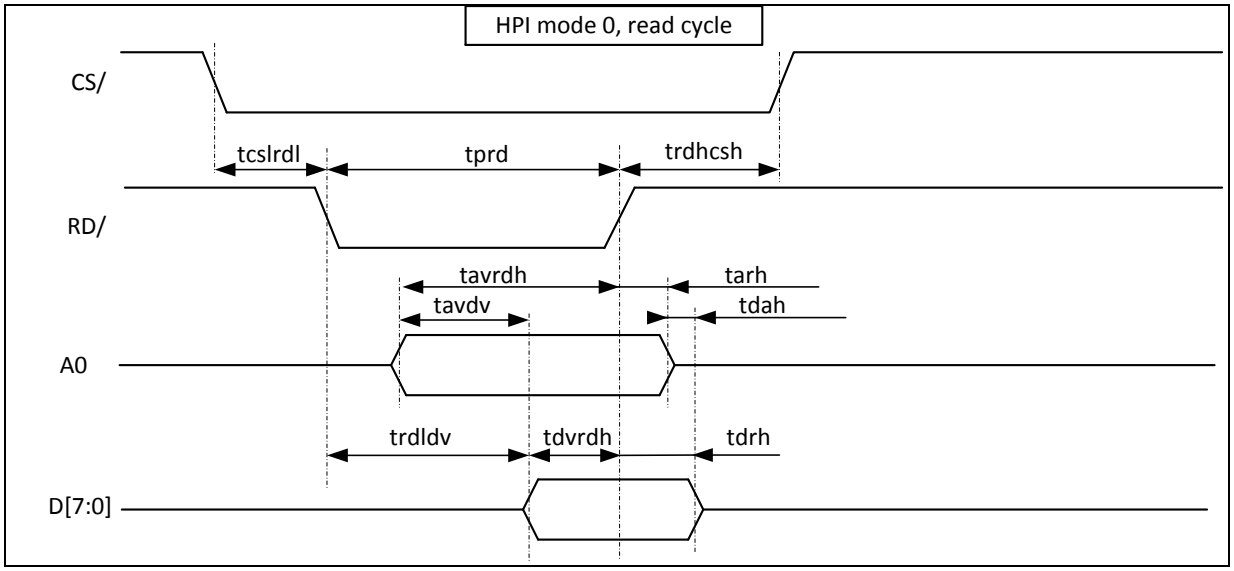
8.4.1. Host Parallel Interface (HPI) mode 0

Pins used in mode 0:

D7-D0: 8-bit Data I/O
CS/: Chip Select from host (input)
A0: Addresses from host for data selection (input)
WR/: Write from host (input)
RD/: Read from host (input)
IRQ (optional): Interrupt Request (output)

This mode is typically used to send MIDI messages or other control data from the Host CPU (master) to the SAM5504B (slave).

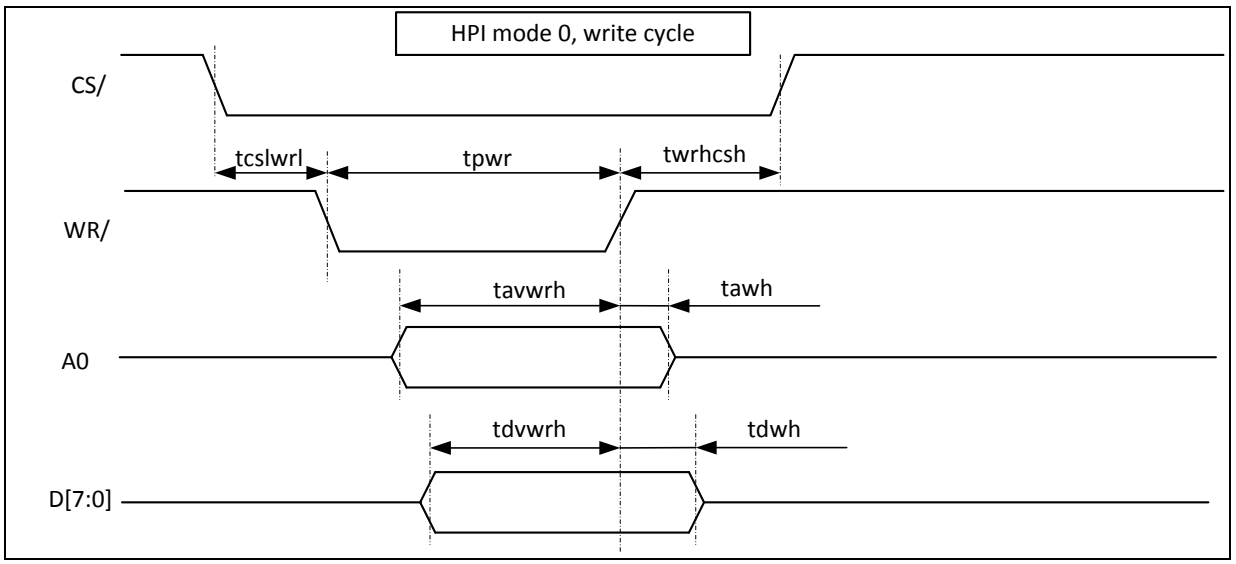
8.4.1.1. HPI mode 0, Timings



Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to RD/ low	tcslrdl	2	-	-	ns
RD/ pulse width	tprd	10	-	-	ns
RD/ high to CS/ high	trdhcsh	3	-	-	ns
Address valid to RD/ high	tavrdh	3	-	-	ns
Address valid to data valid	tavdv	-	-	10	ns
RD/ low to data valid	trdldv	-	-	10	ns
Data valid to RD/ high	tdvrdh	3	-	-	ns
Address out hold from RD/	tarh	3	-	-	ns
Data out hold from RD/	tdrh	0	-	10	ns
Data out hold from address out	tdah	0	-	10	ns

Notes:

1. tcslrdl Min and trdhcsh Min can be reduced to 0 ns if 3 ns are added to tprd Min, tarh Min, tdrh Min, tavrdh Min, tdvrdh Min



Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to WR/ low	tcslwrl	2	-	-	ns
WR/ pulse width	tpwr	5	-	-	ns
WR/ high to CS/ high	twrhcsh	3	-	-	ns
Address valid to WR/ high	tavwrh	3	-	-	ns
Data valid to WR/ high	tdvwrh	3	-	-	ns
Address out hold from WR/	tawh	3	-	-	ns
Data out hold from WR/	tdwh	3	-	-	ns

Notes:

1. tcslwrl Min and twrhcsh Min can be reduced to 0 ns if 3 ns are added to tpwr Min, tawh Min, tdwh Min, tavwrh Min, tdvwrh Min

8.4.1.2. HPI mode 0, IO Status Register

TE	RF	X	X	ID3	ID2	ID1	ID0

Status register is read when A1=0, A0=1, RD/=0, CS/=0

- TE: Transmit Empty: This bit is 1 when nothing is transmitted from SAM5504B to host. If 0, data from SAM5504B to host is pending and IRQ pin is high. Host reading the data with pin A0=0 sets TE to 1 and clear IRQ. TE bit is actually reflecting inverted value of IRQ pin (IRQ/).
- RF: Receiver Full: Host should not write any data or control to SAM5504B if this bit is 1. When 0, then SAM5504B is ready to accept data from host.
- ID[3:0]: these 4 bits are firmware dependant and may be used for defining type of data sent by SAM5504B in case of multiple flows of data.

Host read should be performed with following steps:
a) Nothing to read if IRQ pin is low. First wait for IRQ pin being high
b) Read status (A0=1) to get ID[3:0] (this step is optional if ID[3:0] bits are not used and not defined by firmware)
c) Read data (A0=0) (IRQ goes low at the end of read cycle, on rising edge of RD/ signal)
d) Wait for IRQ pin being high again…
Note: On steps a) and d), if IRQ pin is not connected and not used, host can also read status and wait for TE bit=0

Host write should be done with following steps:
a) Read status (A0=1). If bit RF=0, go to step b). If bit RF=1, read again status till bit RF going to 0.
b) Write new data (A0=0) or new control (A0=1)

Note about step a):
There are two different cases for RF bit being 1:
- RF bit is 1 because FIFO of P16 is full. RF bit will go low again as soon as P16 is reading some bytes of the FIFO in order to have some free space again inside fifo and then is clearing bit 7 (FIFULL) of port 1 (CONTROL/STATUS). This time is firmware dependant.
- RF bit is 1 because previous host write has still not been written into the P16 FIFO. This case can happen if P16 is executing a long instruction. The writing will be indeed performed only when P16 has finished the instruction.

8.5. Serial Slave Asynchronous Interface (UART / MIDI)

The SAM5504B can be controlled by an external host processor through this bidirectional serial interface. Firmware can be downloaded at power-up through this interface.

Pins used:
MIDI_IN1, MIDI_OUT1: UART / MIDI port 1
MIDI_IN2, MIDI_OUT2: UART / MIDI port 2

The serial signals on MIDI_INx and MIDI_OUTx pins are asynchronous signals following the UART / MIDI transmission standard:

Baud rate: programmable up to >400kb/s, typically 31.25 kb/s (MIDI) or 38.4Kbit/s (COM)
Format: start bit (0), 8 data bits, stop bit (1)

8.6. Serial Slave Synchronous Interface

The SAM5504B can be controlled by an external host processor through this unidirectional serial interface. Firmware can be downloaded at power-up through this interface.

Pins used:
SSCLK, SSYNC, SSDIN (input)
SSINT/ (output)

Data is shifted MSB first. SAM5504B samples an incoming SSDIN bit on the rising edge of SSCLK, therefore the host should change SSDIN on the negative SCLK edge.

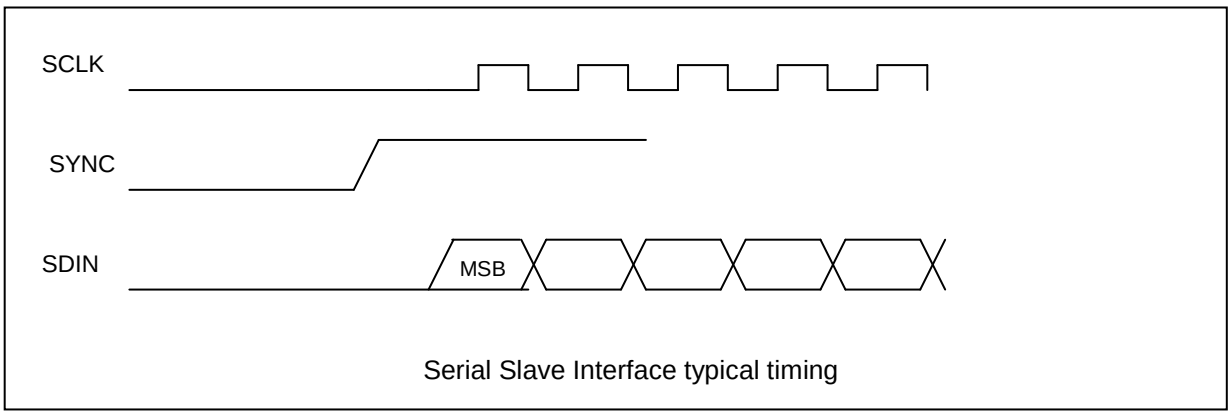
SSYNC allows initial synchronization. The rising edge of SSYNC, which should occur with SSCLK low, indicates that SSDIN will hold MSB data on the next rising SSCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependent. Minimum size is 128 bytes. Host should stop sending data as soon as SSINT/ goes high.

When the FIFO count is below 64, the SSINT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SSCLK frequency is fsck/4 (fsck being the system clock frequency. fsck =1/spck). The minimum time between two bytes is 256 spck.

The contents of the SSDIN data are defined by the firmware.



Serial Slave Interface typical timing

8.7. I²S Digital audio

Pins used:
CLBD, WSBD (outputs): Audio clocks
DABD7-0: Digital audio outputs (8 * 2 channels)
DAAD7-5/3-0: Digital audio inputs (7 * 2 channels)

And optionally
XCLBD0-XWSBD0, XCLBD0-XWSBD0 (inputs): 2 pairs of external clocks for slave mode on DAAD7-5/3-0 inputs.

The SAM5504B allows up to 14 digital audio output channels and 14 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD7-5/3-0 inputs can be individually synchronized with incoming XCLBD and XWSBD signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S or MSB left standard, with up to 24 bits per sample

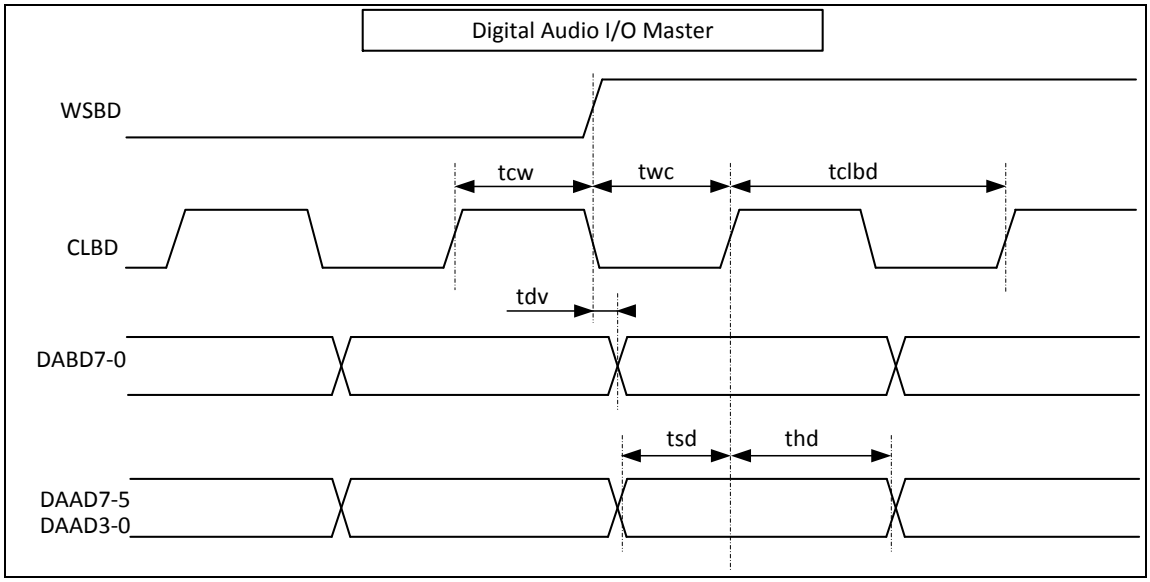
The choice of clock factors is done by the firmware. As an example, table below show some possible clock combinations with 12.288MHz Xtal.

Sampling Rate @ Xtal=12.288MHz	CKOUT freq	CKOUT/WSBD freq ratio	CLBD freq	CLBD/WSBD freq ratio
48kHz	12.288MHz	256	3.072MHz	64
48kHz	24.576MHz	512	3.072MHz	64
96kHz	12.288MHz	128	6.144MHz	64
96kHz	24.576MHz	256	6.144MHz	64
192kHz	24.576MHz	128	12.288MHz	64

Note: WSBD/CLBD ratio is always 64.

8.7.1. Timing

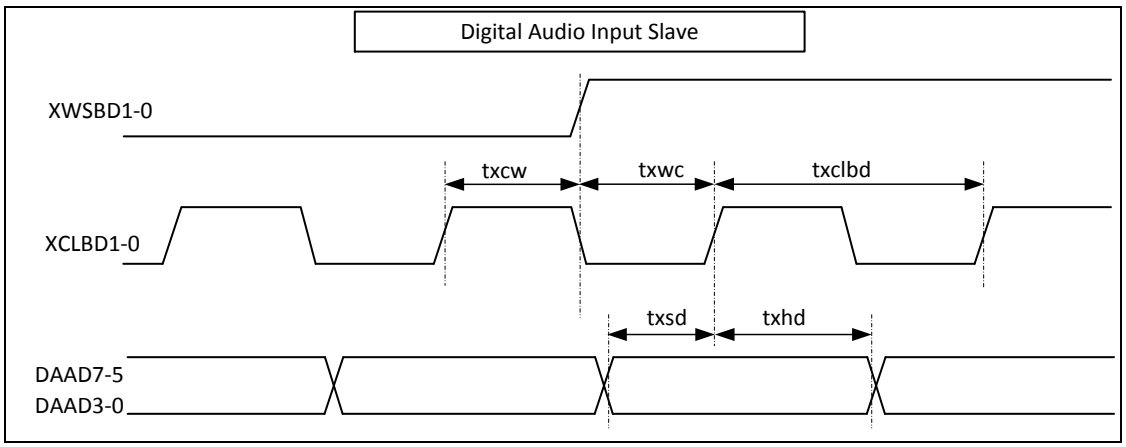
8.7.1.1. Master Mode



cpck is related to CLBD frequency: cpck = 1/(2*CLBD_freq)

Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	cpck -11	-	-	ns
WSBD change to CLBD rising	twc	cpck -11	-	-	ns
DABD valid after CLBD falling	tdv	-11	-	11	ns
DAAD valid prior CLBD rising	tsd	20	-	-	ns
DAAD valid after CLBD rising	thd	20	-	-	ns
CLBD cycle time	tclbd	-	2* cpck	-	ns

8.7.1.2. Slave Mode

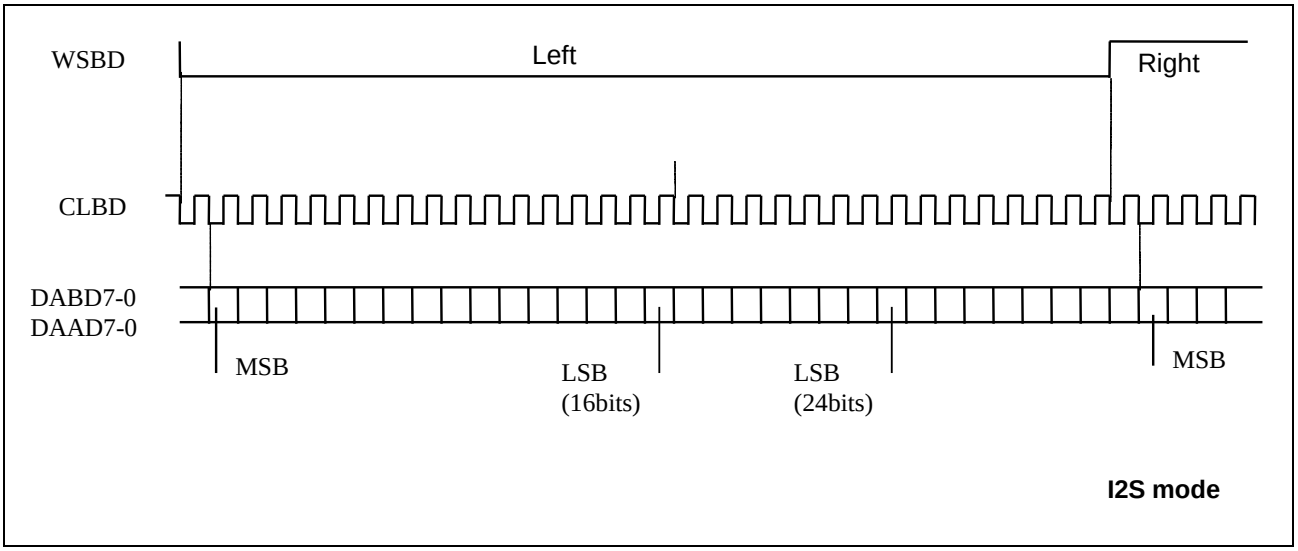


xpck is related to XCLBD frequency: xpck = 1/(2*XCLBD_freq)

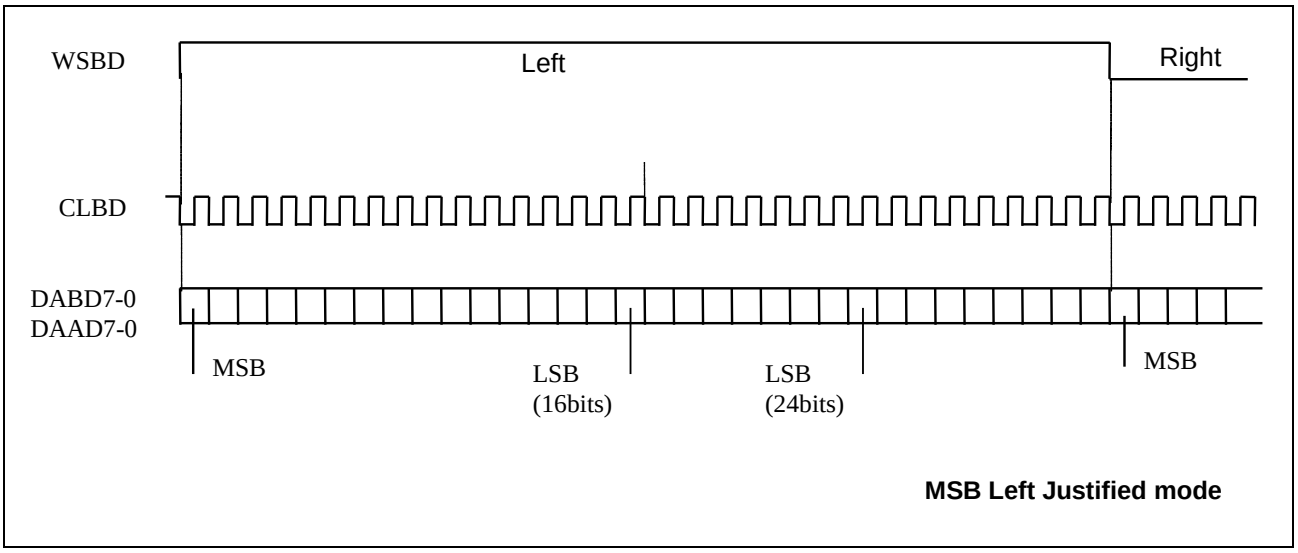
Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	txcw	20	-	-	ns
WSBD change to CLBD rising	txwc	20	-	-	ns
DAAD valid prior CLBD rising	txsd	20	-	-	ns
DAAD valid after CLBD rising	txhd	20	-	-	ns
CLBD cycle time	txclbd	-	2* xcpck	-	ns

8.7.2. Digital Audio Format

SAM5504B can generate I2S or MSB Left justified digital audio format. Master Clock CLBD can be 128xFs, 256xFs, 512xFs, 192xFs, 384xFS or 768xFs. Format and clock ratio are selected by firmware.



I2S mode



MSB Left Justified mode

8.8. SPDIF Digital audio

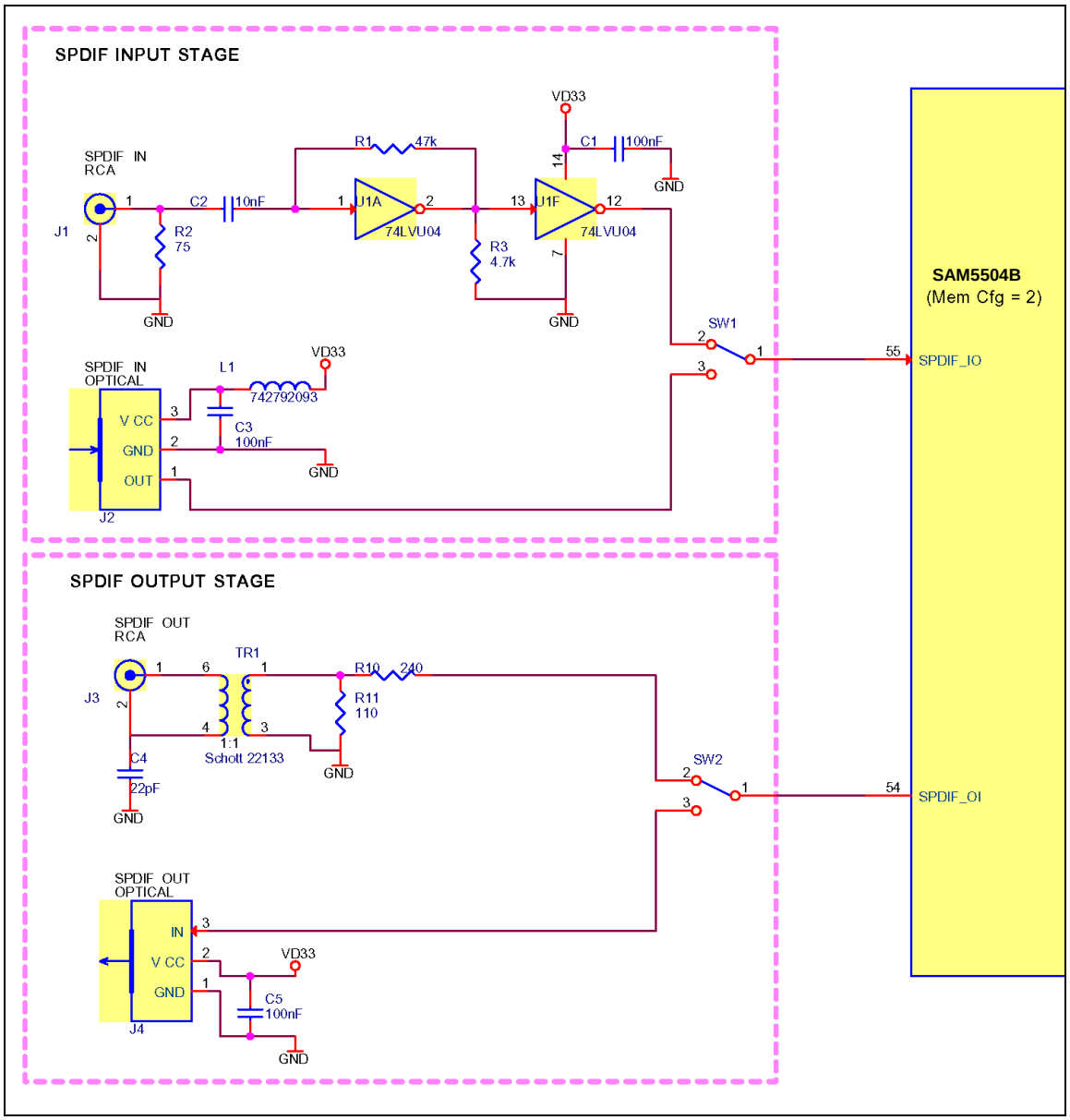
The SPDIF Digital Audio Interface Controller implements the IEC60958 interface features (commonly known as Sony/Philips Digital Interface), a unidirectional and self-clocking interface for connecting digital audio equipment using the linear PCM coded audio samples.
Receiver and Transmitter modes are supported at the same time.

Pins used:
SPDIF_IO: Serial data input (by default)
SPDIF_OI: Serial data output (by default)

Data mode capabilities:
- Sample rate from 3kHz to 192kHz
- 24 bit per sample

8.8.1. Reference Schematic

Schematic below is example design for SPDIF IN and OUT interface with SAM5504B.



8.9. USB 2.0 Ports

SAM5504B offer one USB 2.0 (High-Speed) ports.
It can be can be used as Device, Host or Dual Role.

Pins used:

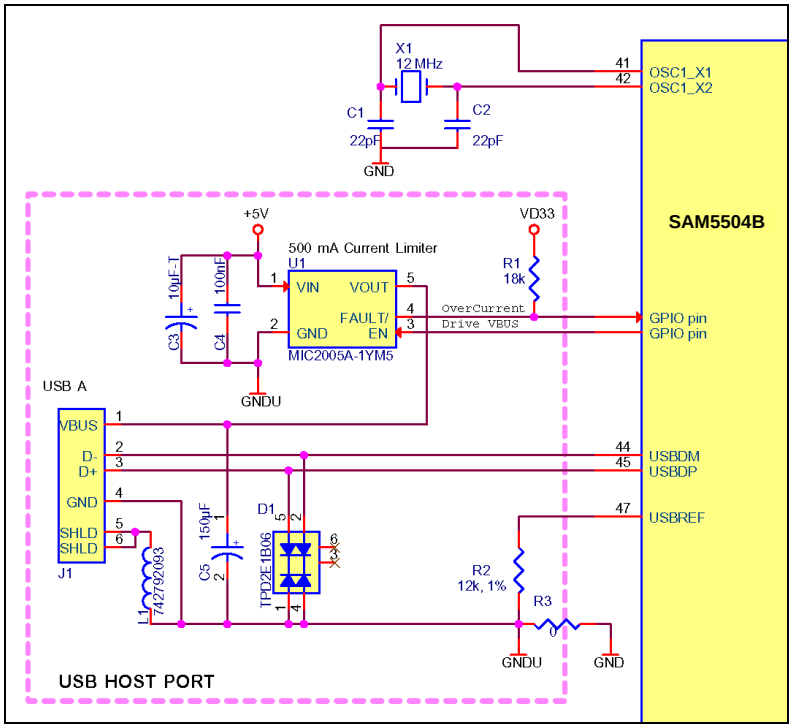
OSC1_X1-OSC1_X2:	12MHz Crystal connection for USB and system boot
USBDM-USBDP:	Differential analog IO 0
USBREF:	Connection to 12kΩ ± 1% reference resistor

8.9.1. USB Device Port

Schematic below can be used as reference for application with USB Device Port

8.9.2. USB Host Port

Schematic below can be used as reference for application with USB Host Port



9. Audio Synchronization

9.1. Synchronization on external audio devices

In professional applications, it can be decided to synchronize SAM5504B audio processing on external audio flow(s) from USB or SPDIF interfaces. Another professional feature is synchronization on external word clock.

9.1.1. Principle

- Audio clock frequency is extracted from incoming audio flow or from external word clock and is compared with frequency currently used for internal audio processing.
- Comparison result is used to control the internal PWM generator.
- PWM generator output is filtered, and then, can drive an external VCXO.
- VCXO clock output is used as master clock for internal audio processing.

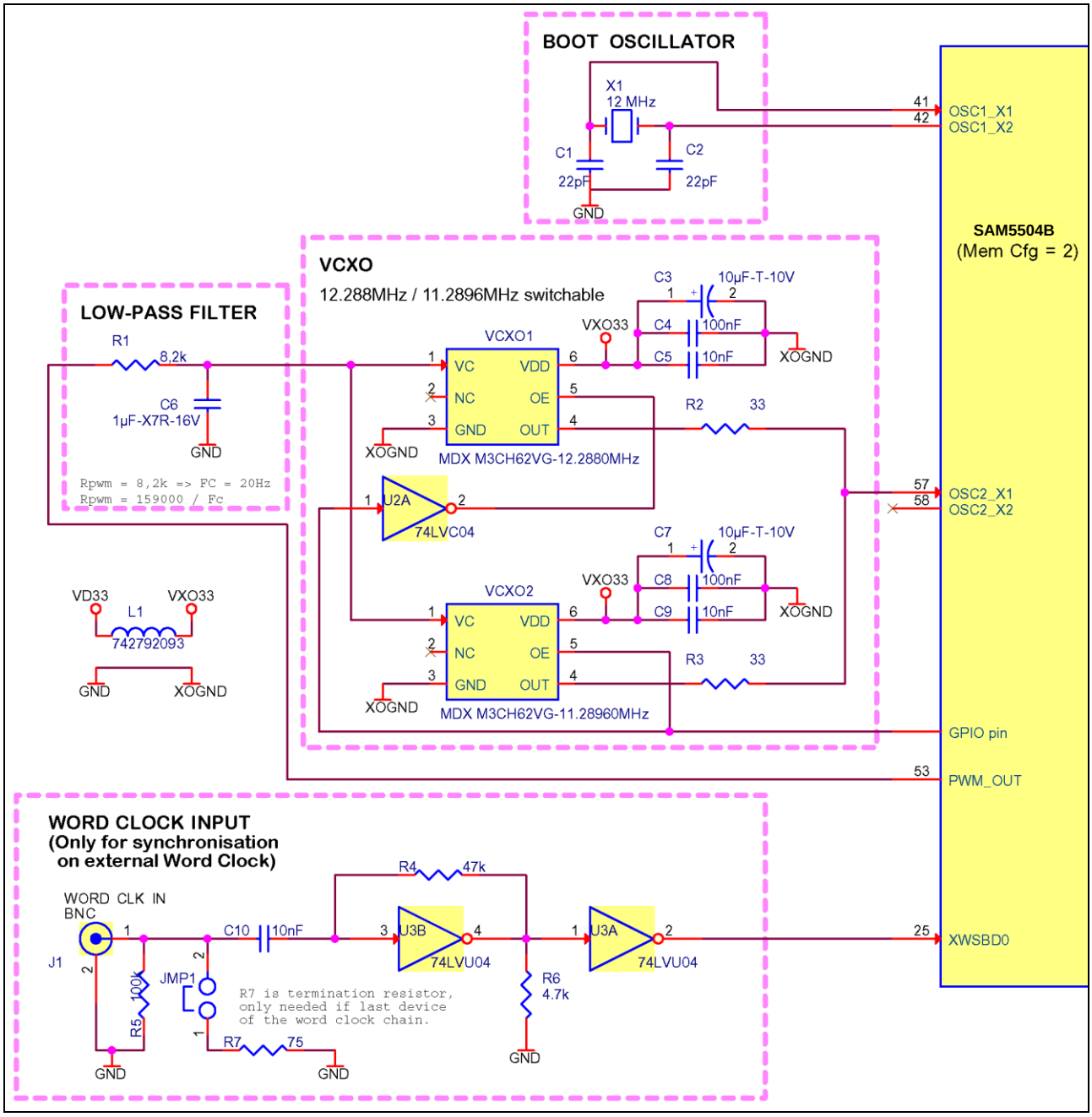
As a result, clock frequency for internal audio processing is perfectly enslaved to incoming audio flow.

Pin used:

OSC1_X1, OSC1_X2:	Connection to 12MHz crystal for USB and system boot
X1:	Clock input for audio system clock from VCXO
PWM:	PWM output
XWSBD0 (optional):	Input for external Word Clock

9.1.2. Reference schematic

Schematic below can be used as reference for synchronization on external audio flowing and optionally on external word clock.

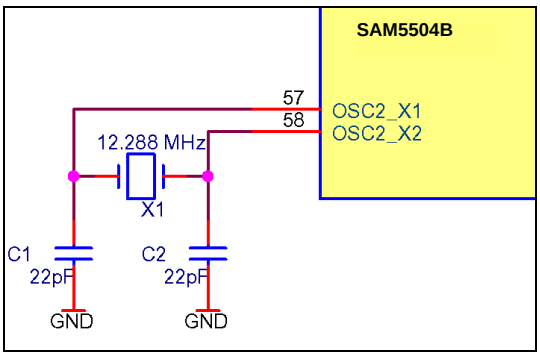


- At start-up system runs on main oscillator connected to OSC1_X1/X2 inputs (typ. 12MHz)
- When environment is stabilized, firmware switches system and audio clock source from main oscillator to second oscillator input OSC2_X1 driven by VCXO clock.

Notes:
- PCB design around VCXO is sensitive. See VCXO manufacturer relative application notes.

10. Recommended Crystal Compensation

10.1. OSC2_X1 – OSC2_X2



C1 and C2 should be chosen in range 12pF-27pF. Different values lead to different oscillation characteristic and can be selected based on board layout considerations.
External feedback resistor should be avoided because there is an internal feedback resistor.

10.2. OSC1_X1 – OSC1_X2

Crystal connection on OSC1_X1-OSC1_X2 follows the same off-chip components recommendation than crystal connection on OSC2_X1-OSC2_X2

11. Reset and Power Down

During power-up, the RST/ input should be held low until the core is stabilized in reset state, which takes 10ms Max.
After the low to high transition of RST/, following happens:

- Oscillator OSC1 is started
- P16 program execution starts in built-in ROM
- PLL is started and stabilized after 2.8 ms typ
- P16 application program loading starts.

If RST/ is asserted low then the crystal oscillators and PLLs will be stopped.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256
- ADC can be disabled
- Controllers for USB and memories can be individually switched off

11.1. Power-up sequence

At power-up the following sequence is executed:

1. STIN is sensed. If HIGH, then the built-in debugger is started.
2. If MC0 bit was preprogrammed it is read from eFuse. Otherwise MC0 pin is sensed and corresponding Memory Config is set.
3. ROM boot tries to identify source for firmware. For that it tries to find “DR” marker for Dream firmware. This step is done in slow mode (PLL not started). During this step, rom boot set the minimum of primary functions to avoid any potential conflict of some pins. Accesses to memories are done with longest access time, most simple protocol (accessing for example Quad SPI memory in single mode rather than quad mode). ROM boot searches source in following order:
   a) Quad-SPI NOR Flash
   b) Multi-Purpose SPI
4. If valid firmware has not been found, firmware download from a host processor is assumed into internal RAM (40k x 16 max) through 8-bit Parallel (if eFuse 14 not blown, default), Serial Slave Synchronous (if eFuse 14 blown) or Serial Slave Asynchronous (MIDI_IN1) port.

<u>If Host CPU is connected on 8-bit Parallel Interface (eFuse 14 not blown, default):</u>

a) The byte 0ACh is written to the host. The host checks status and can recognize that the chip is ready to accept program download.
b) The host sends the Boot_Info table (low byte first, 20 * 2 bytes). Boot_Info table contains info on firmware size, primary and secondary functions setting, memory and software config. The Boot_Info table is generated by SamVS, and is located in the firmware binary file at word addresses 1-20.
c) SAM5504B sends ACh when initializations are ready
d) The host sends the SAM5504B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
    a. "DownLoadSize" is defined in the Boot_Info table at word address 3.
e) The byte 0ACh is written to the host. The host checks status and can recognize that the chip has accepted the firmware.
f) SAM5504B starts the firmware.

Note: Be aware that at boot time the IRQ signal is not used, the Host CPU must read the port status register (TE/RF bits) before sending or reading a data byte to/from SAM5504B via 8-bit parallel port.

If Host CPU is connected on Serial Slave Synchronous Interface (eFuse 14 must be blown):

a) The host sends the Boot_Info table (low byte first, 20 * 2 bytes, see description above).
b) The host sends the SAM5504B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
c) SAM5504B starts the firmware.

Note:
For debug purpose of the download through Serial Slave Synchrounous interface, if eFuse 15 is blown, the acknowledge bytes ACh can be checked on the MIDI_OUT1 pin.

If Host CPU is connected on Serial Slave Asynchronous Interface (MIDI_IN1):

Download through MIDI_IN1 is always available (there is no eFuse to be blown). However, the acknowledge bytes ACh are sent on MIDI_OUT1 only if eFuse 15 is blown.

a) If eFuse 15 is blown, the byte 0ACh is sent on MIDI_OUT1 to the host.
Note: this first ACh byte may be difficult to be recognized by host because during power-up the MIDI_OUT1 pin is in undefined state and host may receive many invalid midi data before receiving this ACh byte. This first ACh byte is more intended for debug purpose or scope checking.
b) Host sends at 38.4Kbit/s the 2 bytes 52h and 44h on MIDI_IN1
Note: SAM5504B automatically disables the download through MIDI_IN1 if the 2 first bytes received are not 52h and 44h.
c) Then host sends at 38.4Kbits/s the Boot_Info table (low byte first, 20 * 2 bytes, see description above). A new baud rate is defined in the Boot_Info table at word address 4.
d) If eFuse 15 is blown, SAM5504B sends ACh on MIDI_OUT1 (at new baud rate).
e) The host sends at new baud rate the SAM5504B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
f) If eFuse 15 is blown, the byte 0ACh is sent to the host (new baud rate).
g) SAM5504B starts the firmware.

Note: When using download through MIDI_IN1, the 2 other host interfaces must not be active during download:
- if eFuse 14 not blown (host 8-bit parallel interface): pin CS/ (or pin WR/) of 8-bit parallel interface must be high.
- if eFuse 14 blown (Serial Slave Synchronous interface): clock pin SSCLK of Serial Slave Synchronous interface must be idle

11.2. Pin status in Power-down mode

Table below shows the status of each I/O pin in Power-down mode (RST/ Low)

Pin name	Status in Power-down mode
VIN	ANA IN
RST/	IN driven Low
TEST	IN with Pull-down resistor
STIN	IN with Keeper resistor
STOUT	IN with Pull-up resistor
CKOUT, CLBD, WSBD	IN with Keeper resistor
All other I/O pins	IN with Keeper resistor

Note:

- Keeper resistor can be pull-up or to pull-down resistor. This will depend on logic state at the pin where it is connected when switching to Power-down mode.
    - If logic state is ‘Low’ when entering Power-down mode, keeper resistor will be pull-down
    - If logic state is ‘High’ when entering Power-down mode, keeper resistor will be pull-up

12. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

12.1. GND, VD33, VC12, VD12 distribution, decoupling

All GND, VD33, VC12, VD12 pins should be connected. A GND plane is strongly recommended. The board GND, VD33, VC12 and VD12 distribution should be in grid form.

Recommended VD12 decoupling is 0.1µF at each VD12 pin of the IC with additional 10µFT on two opposite sides

VC12 pin requires 10µFT +100nF.

Recommended VD33 decoupling is 0.1µF at half of VD33 pins. 10nF should be connected at the other half of VD33 pins. 10µFT should be also added on two opposite sides.
VD33R requires a single 10µFT decoupling.
VD330 requires a single 100nF decoupling.
VD33U requires 10µFT+100nF+10nF capacitors.

12.2. Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

12.3. Busses

A ground plane should be implemented below the D7-D0 bus, which connects both to the host and to SAM5504B GND.

12.4. ESD and EMI

Below are some tips that allow reaching good protective level again EMI and ESD with SAM5504B. This list is no exhaustive.

- Equipotentiality of the ground plane is a major point to avoid weakness against EMI. The 4 layer design is the best solution. When 2 layer design, the unused zones of the component side should be filled with ground planes connected with a lot of through holes to the ground plane of the solder side.

- High speed clock and signals trace should be short and shielded. Serial resistor or RC filter can be added close to the source to filter harmonics.

- Main power supply, before regulators should be protected with T filter like Murata NFM41PC204F1H3 and serial choke coil like LQH43CN220K03

- Connectors should be protected. EMI filters like Murata NFM21CC102R1H3 should be implemented on the clock and data lines, close to their connection on the connectors. Power supply lines can be protected with Murata BLM21RK102SN1 or Wurth 742792093.

- Each power supply pin of SAM5504B and of all active components should be decoupled with 100nF X7R capacitor and 470pF NPO or COG capacitor. A 10µF capacitor should be added close to the SAM5504B Xtal.

- Each active component should be isolated from the main power supply with a serial inductor on its power supply lines. Murata BLM21RK102SN1 or Wurth 742792093 can be used for this.

- Address, Data, Chip select, Reset signals for SAM5504B should be isolated from their environment with serial 33 Ohm resistor close to SAM5504B.

- Data, clock lines signals for DAC should be isolated from their environment with serial 22 Ohm resistors close to the DAC.

- On sensitive lines like Reset, 470pF NPO or COG capacitor can be added, close to SAM5504B.

13. Product development and debugging

Dream provides an integrated product development and debugging tool “SamVS”.
SamVS runs under Windows (WinXP and up). Within the environment, it is possible to:

- Edit
- Assemble / Compile (C Compiler for P16XT included) and build firmware binary file
- Debug on real target (In Circuit Emulation)
- Program external Quad-SPI NOR Flash, DataFlash or EEPROM on target.

Separated tools allowing programming the internal eFuses of SAM5504B, e.g. “ProgSam” provided by Dream for in-circuit programming of eFuses and Firmware/sound bank.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using serial communication at 57.6kb/s. Dream provides a USB debug interface (5000DBG-IF) for easy use.

A library of frequently used functions is available within the SamVS-C development package (5504xx-C-PDK). Thus time to market is optimized by testing directly on the final prototype.

Dream engineers are available to study customer specific applications.

Dream Contact

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