SAM5704B

AUDIO & MUSIC MULTI-DSP PROCESSOR

Key features

- **Dream DSP Array of 4 new 24bit/56bit DSP cores** (P24XT) supporting 56bit MAC operations (200M MAC/sec), vector processing, double precision instructions and offering a rich set of hardware accelerated macro-instructions (including 48x48bit multiply or double precision bi-quad filter)
- New highly **speed optimized 16bit CPU** (P16XT) running at 200MHz, with optimized instruction set for C compiler, interrupts, new fast 32-bit instructions, 512Kword max. program code size
- Built-in 1kbit eFuse for configuration and security (program code and sound bank protection)
- Built-in configurable fast **Data/Effect RAM up to 32Kx24** (or 48Kx16), + 8Kx24 DSP RAM
- Built-in configurable fast Program Code/Cache RAM, on-the-fly code decryption
- Multi-channel DMA for fast data transfers to external memories, supports circular buffers and transparent 24- to 16-bit transformation
- External memories: parallel or serial configurations through 1 or 2 separated ports with flexible configurations (NOR Flash + SRAM/SDRAM, 8bit SLC NAND Flash (with ECC) + SRAM/SDRAM, Quad-SPI-NOR), up to 512MByte addressing space for NOR Flashes, **8GByte for NAND Flashes**
- On-the-fly wave sample decryption (AES encryption format with high security)
- 8-bit parallel slave Port capability for external Host control and fast data transfer
- Multi-purpose SPI interface (single or Quad-SPI, mode 0) for Serial Flash, SD-Card…
- Serial MIDI IN/OUT (UART) interface (optional 2nd I/F)
- **USB 2.0 High Speed** port (HOST, DEVICE or Dual-Role) for USB-Disk (flash drive) or AudioClass compliant Audio/MIDI interface function, and other USB functions
- **10/100 Mbps Ethernet MAC** with RMII interface to external PHY
- Up to **192kHz S/PDIF** interface (IEC60958) with clock recovery (concurrent IN/OUT)
- On-die synchronization PWM mechanism controlling external VCXO for audio streaming from external sources
- Up to 16 Audio channels IN / 16 Audio channels OUT, most Audio IN can be used in clock slave mode
- Direct connection to velocity keyboards (various types), LEDs, switches, sliders/potentiometers/ modulation wheels, LCD or Graphic Display and others
- Watchdog, Timers, Power reduction modes, unused primary interfaces can be used as GPIOs
- 128-pin LQFP package

Typical applications

- Low cost Digital Pianos & Keyboards
- Effect devices, Speaker processing, USB Audio Interfaces…

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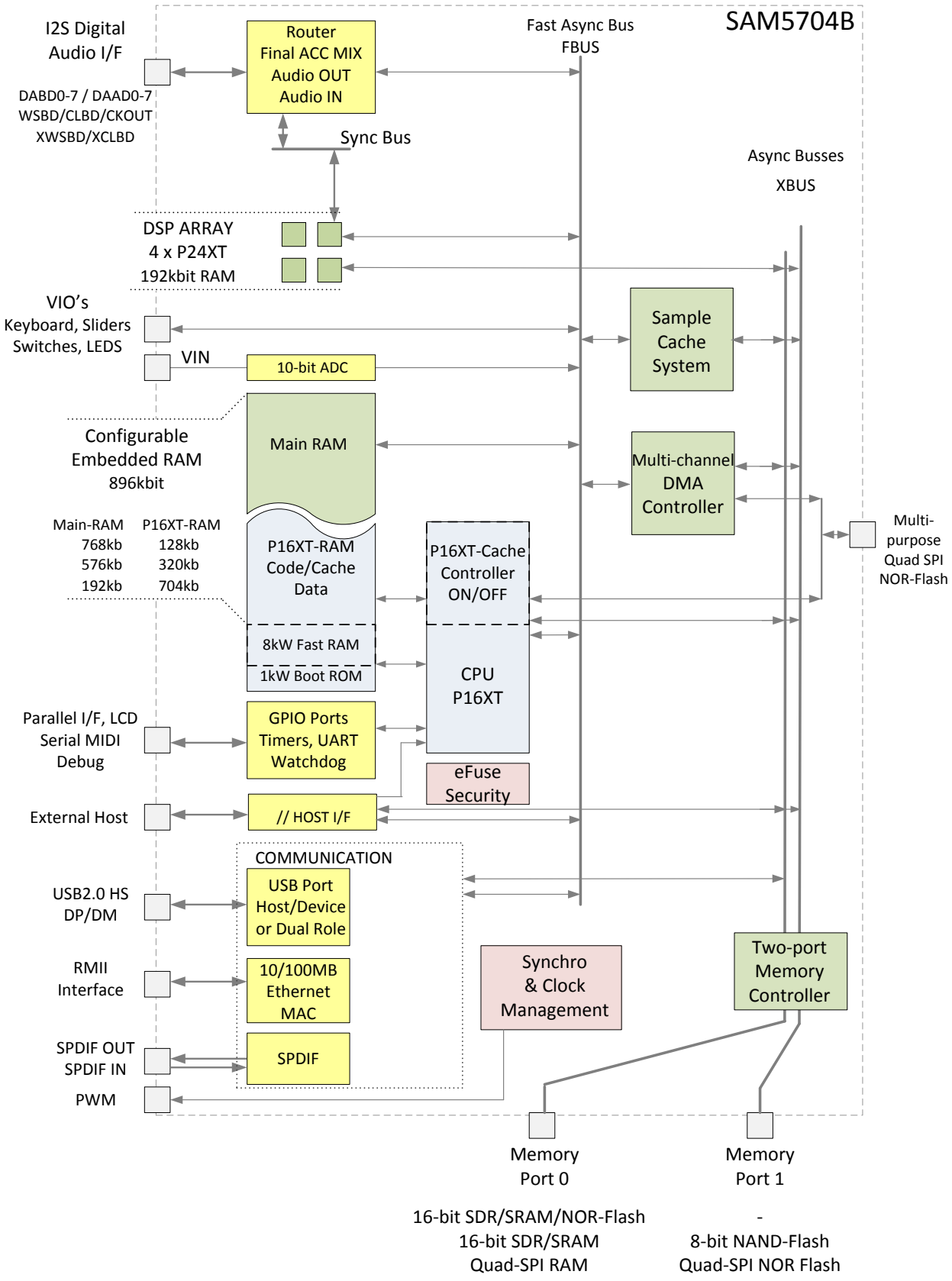
1. SAM5704B Internal Architecture

1.1. Block Diagram



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1.2. Overview

Based on a multi-layer architecture, the new family of DREAM's Audio & Music processors (SAM5000) is built around a new highly speed optimized 16-bit CPU (P16XT) and a configurable array of hardware accelerated 24-bit DSP cores (P24XT).

A Sample Cache System dedicated to sound synthesis allows SAM5000 processors to reach high levels of polyphony whatever the memory type used for sound bank storage. Moreover, this solution allows on-the-fly decryption of waves protected with strong AES(*) encryption.

The processing of delay lines in external memory is hugely facilitated with the integration of a multi-channel DMA controller. This controller performs fast memory-to-memory data transfers with some key features: burst modes and circular buffer structures are supported and data are automatically re-formatted (24-bit↔16-bit) when transfers are done from internal to external memories. Transfers can be done in parallel on several channels without requiring any assistance of the CPU or DSP cores.

The SAM570B is part of the new generation of DREAM's audio & music processors and automatically inherits all above features. With an array of 4 P24XT DSP cores, the SAM5704B is delivered in a cost-efficient 128-pin QFP package. It is intended to low-cost keyboard, effect and professional audio applications.

In addition to a large variety of communication interfaces (USB 2.0 HS port, Ethernet MAC controller, S/PDIF IN/OUT…), the SAM5704B has two memory ports supporting various, parallel or serial, memory types. Up to 6 different memory configurations can be defined with pull-resistors externally connected to dedicated pins. Memory configuration is read by boot program at power-up from dedicated pins or fuse bits.

The SAM5704B includes a 24-bit Audio Router and supports up to 16 Audio Channels IN & OUT. Depending on primary functions in use, digital audio signals can be accessed via primary or secondary IO pads. Most of the IO pads that are not used for primary functions remain available for secondary functions or for firmware programmable IO functions (Versatile IO's or GPIO's).

The SAM5704B can handle up to 176 switches (organized in matrix form) and 88 LEDs (in a time multiplexed way) through versatile firmware programmable IO pads. Keyboard and switches scanning tasks can be fully customized in one dedicated P24XT, making the SAM5704B directly compatible with most of velocity keyboards. Similarly, LCD or graphic displays can be directly connected to programmable IO's and controlled by the P16XT.
A built-in ADC allows connecting continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc.

A built-in 1kbit eFuse provides a plenty of irreversible One-Time-Programmable bits for the storage of configuration parameters, decryption keys and other security purposes. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5704B.

(*) AES is the worldwide most used symmetric-key algorithm.

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1.3. DSP Array – 4 * P24XT

The SAM5704B is built around an Array of 4 new 24-bit DSP cores (P24XT).

Similarly to previous generation, each P24XT DSP core includes a 2k x 24 RAM and a 2k x 24 ROM. The RAM contains both data and DSP instructions, while the ROM contains typical coefficients such as FFT cosines and windowing and micro-code for hardware accelerated micro-instructions.

The P24 sends and receives audio samples through the Sync Bus at the frame rate (typically, 48kHz frame period = 2048 cycles at 98.8 MHz). For the transfer of all other data, the P24XT is able to communicate in an asynchronous way through Async Busses. P24XT memories can be accessed through the Async Bus by others.

A lot of operations can be performed with much more precision with new P24XT core.
For single-precision operations:

- Programmable 24-bit fixed format: 1.0.23, 1.2.21, 1.8.15 or 1.15.8
- 56-bit MAC unit with 24-bit x 24-bit multiplication + 8 guard bits to prevent overflow issues

For double-precision operations:

- Programmable 48-bit fixed format: 1.0.47, 1.2.45, 1.8.39 or 1.15.32
- Large set of 48-bit Double Precision (DP) operations

The P24XT DSP core also offers hugely improved performances with a new and rich set of hardware accelerated macro-instructions:

  - ADD, MUL, MAC operations on vectors can be performed with only one macro-instruction, address pointers being self-incremented
  - ring buffer structures are supported in several vector instructions
  - several arithmetic operations are available: SIN, COS, DIV, LN, EXP, …
  - Operations on complex values in single and double precision
  - Polynomial calculation in single and double precision
  - Optimized filtering instructions: 1^{st} & 2^{nd} order filters, programmable number of taps, single or double precision

Based on polynomial interpolation, up to 27 sounds (at typical 48kHz frame clock) with high quality filtering can be synthesized within one P24XT and up to 50M of 56-bit MAC operations can be performed per second.

1.4. Sync Bus

The Sync Bus transfers audio samples on a frame basis, typical frame rates being 44.1, 48, 96 & 192 kHz. Each frame is divided into 32 time slots. Each slot is divided into 8 bus cycles. Each P24XT is assigned a hardwired time slot (16 to 31), during which it may provide 24-bit data to the bus (up to 8 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 15 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

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1.5. Async Busses

As shown in the general block diagram, several 24-bit Async Busses can be accessed by most of masters (P16XT, P24XT, DMA controller,…) in a parallel way. Two busses XBUS0 & XBUS1 give access to external memories.

1.6. Enhanced 16-bit CPU – P16XT

The SAM5704B operates under the control of a new highly speed optimized 16-bit CPU (P16XT).

The key features of the P16XT are the following:

- Operating frequency = 196.6 MHz
- New instructions including 32 bit data handling and 32x32 multiply
- Maximum executable program size = 512k words
- Backward compatibility with previous P16 products and optimized instruction set for C-compiler
- Interrupt handling: 3 interrupt signals, 32 sources with programmable Mask, Polarity & Triggering mode

A tightly coupled code/cache memory allows the P16XT to fetch code lines with reduced latency when needed. This memory can be either used as code memory when the whole firmware can be stored in internal memory or as cache memory (n-Way Set Associative Cache System) in other cases. The internal code/cache memory is loaded during the boot sequence (at power-up) by P16XT ROM boot program.

By default, the code/cache memory has a size of 256kbits (16k*16). Depending on performance requirements, the distribution of internal memory between code/cache and data/effect partitions can be modified as explained in the next paragraph.

The P16XT ROM holds the boot program as well as a debugger which uses a dedicated asynchronous serial line.

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1.7. On-chip memory

Besides distributed memory in P24XT DSP cores (4 * 2Kx24-bit RAM for a total of 192kbits) and in communication controllers, the SAM5704B offers 896k bits of on-chip memory. One part of this memory (P16XT-RAM) is reserved for direct access by the P16XT (tightly coupled code/cache memory). The second part of this memory (MAIN-RAM) is used as data memory and can be accessed by any master through the asynchronous bus.

The memory partitioning is configurable by firmware. The memory space is divided into 4 banks:

- Bank 0 has a size of 128kbits and is accessed by P16XT only.
- Bank 1 has a size of 192kbits and can be either used as code/cache memory for P16XT or as main data memory
- Bank 2 has a size of 384kbits and can be either used as code/cache memory for P16XT or as main data memory
- Bank 3 has a size of 192kbits and is always used as main data ram

		RAMCFG='00'		RAMCFG='01'		RAMCFG='10'	
		P16XT RAM	Main RAM	P16XT RAM	Main RAM	P16XT RAM	Main RAM
Bank0	128 kbits	8kx16	-	8kx16	-	8kx16	-
Bank1	192 kbits	-	8kx24	12kx16	-	12kx16	-
Bank2	384 kbits	-	16kx24	-	16kx24	24kx16	-
Bank3	192 kbits	-	8kx24	-	8kx24	-	8kx24
Total		128kbits 8kx16	768kbits 32kx24	320kbits 20kx16	576kbits 24kx24	704kbits 44kx16	192kbits 8kx24

1.8. Multi-channel DMA controller

The DMA controller is intended to perform high-speed memory-to-memory data transfers without using CPU resources: blocks can be copied from one source address to one destination address with a specified length, while both source and destination addresses are self-incremented. Taking advantage of the multi-layer architecture, this module can operate on several channels in parallel. Moreover, the DMA controller is able to automatically perform 24-bit to 16-bit transformation when data blocks are transferred from internal to external memories. For making the handling of delay lines easier, circular buffers are also supported.

Main features:

- The DMA controller has 4 channels
- programmable block length and source & destination addresses
- supports word and burst transfers
- supports ring buffers
- transparent 24-bit to 16-bit transformation

1.9. Sample Cache System

Thanks to its sample cache system, the SAM5704B can support up to 81 voices of polyphony with sound banks stored in SDRAM, NOR-Flash, NAND-Flash or Quad-SPI NOR. With NAND-Flash, cache memory must be extended in external SRAM/SDRAM.

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1.10. Two-port memory controller

The two-port memory controller enables the SAM5704B to interface with various, parallel or serial, memory types:

Config	*Port0*	*Port1*	*KBD Interface*
1	16-bit SDRAM + NOR Flash	-	No
2	16-bit SRAM + NOR Flash	-	No
3	16-bit SDRAM	8-bit SLC NAND Flash (with ECC)	No
4	16-bit SRAM	8-bit SLC NAND Flash (with ECC)	No
5	16-bit SRAM	-	No
6	QuadSPI-SRAM	QuadSPI-NOR	Yes

Memory configurations are defined with pull-resistors externally connected to dedicated pins and are read by boot program at power-up from dedicated pins or fuse bits.

Configuration 6 with low pin-count serial memory interfaces is dedicated to keyboard applications.

For the storage of sound banks, address lines support

- up to 2 x 256MBytes of non-volatile NOR Flash memory
- up to 2 x 4GBytes of non-volatile NAND Flash memory

The two-port memory controller handles transfer requests initiated by masters like P16XT CPU, P24XT DSP cores, DMA controller, Sample cache system or other communication controllers through both XBUS asynchronous busses.

Control registers are accessed by the P16XT for defining configuration and optimizing frequency and latency parameters. Burst transfers are always initiated when possible.

1.11. Router: final ACC, MIX, audio out, audio in

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 16 channels of audio in and 16 channels of audio out are provided (8 stereo in/out, I2S or MSB Left format). The stereo audio in channel may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

1.12. External Host Interface

The Host Parallel Interface is used for fast read/write transfers between an external host processor and the SAM5704B. E.g. it allows an external host to be a master for fast data transfer to SAM5704B connected memories (the handshake protocol for the fast data transfer is driven by the firmware).
This module is connected internally to asynchronous busses.

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1.13. Versatile I/O's and GPIO's

Most of the IO pads, when not used for primary (or secondary) specific functions, remain available as firmware programmable IO pads. Programmable IO functions are divided into 2 categories:

- Versatile IO's when they can be controlled through asynchronous busses by either P16XT or P24XT cores for keyboard scanning, sliders, switches and LED's control.
- General Purpose IO's (GPIO's) when accessible by the P16XT only for functionalities like LCD Display control, …

1.14. High-speed USB 2.0 Port

USB Port allows the SAM5704B to connect it directly to

- an USB host such as a PC in device mode
- an USB device such as a mass storage USB key in host mode.
- USB Port supports also dual-role mode

USB Port has PHY on-die.

1.15. 10/100Mbit Ethernet MAC

The SAM5704B offers the capability to be directly connected to a network by way of an embedded Ethernet MAC. The controller supports both 10M and 100M bits/sec. Low-pin count RMII protocol is used for connection to external PHY.

1.16. S/PDIF – Sony/Philips Digital Interface

The S/PDIF audio module allows the SAM5704B to receive and transmit digital audio concurrently. The SAM5704B provides one single S/PDIF receiver with an input signal and one S/PDIF transmitter with another output signal.

For synchronization purposes, the audio clock can be recovered from the incoming audio stream.

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1.17. Synchronization and clock management

Depending on the application, the SAM5704B supports 3 clock sources (OSC1, OSC2 & VCXO) for the generation of the reference clock (see table below) and 2 programmable PLL. With a crystal at 12.288MHz, the main PLL generates a clock at 393.2 MHz (32*12.288MHz). This high-frequency system clock is optionally divided through programmable dividers to generate several slower control clocks. Most of internal clocks can be stopped individually for flexible power optimization.

For audio streaming applications, the SAM5704B is able to behave as a slave. Synchronization to an external clock, extracted from input audio streaming for example, can be achieved by controlling an external VCXO with built-in PWM signal. Re-synchronized clock from VCXO can be used as 3rd clock source. In this case, the SAM5000 does use the clock from OSC1 (12MHz) during the start-up period.

Clock Mode	USB/ Eth in use	Description	OSC1 (MHz)	OSC2 (MHz)	Audio Source Clock (MHz)	Typical (*) frame clock (kHz)
0	Yes	Single-Xtal 12MHz-USB/Eth	12	NU	12	46.875
1	No	Single-Xtal 12.288/11.2896MHz-Audio	12.288 11.2896	NU	12.288 11.2896	48 44.1
2	Yes	Two-Xtal 12MHz-USB/Eth + 12.288/11.2896MHz-Audio	12	12.288 11.2896	12.288 11.2896	48 44.1
3	Yes	Two-Xtal 12MHz-USB/Eth + VCXO	12	VCXO	VCXO	Ext. frame frequency

(*)SAM5000 supports 46.875kHz, 48/44.1KHz, 96/88.2KHz and 192/176.4KHz sampling rates

1.18. eFuse and security

A built-in 1kbit eFuse provides a plenty of irreversible One-Time-Programmable bits for the storage of configuration parameters, decryption keys and other security purpose data. AES-protected sound banks and firmware can be decrypted on-the-fly within the SAM5704B.

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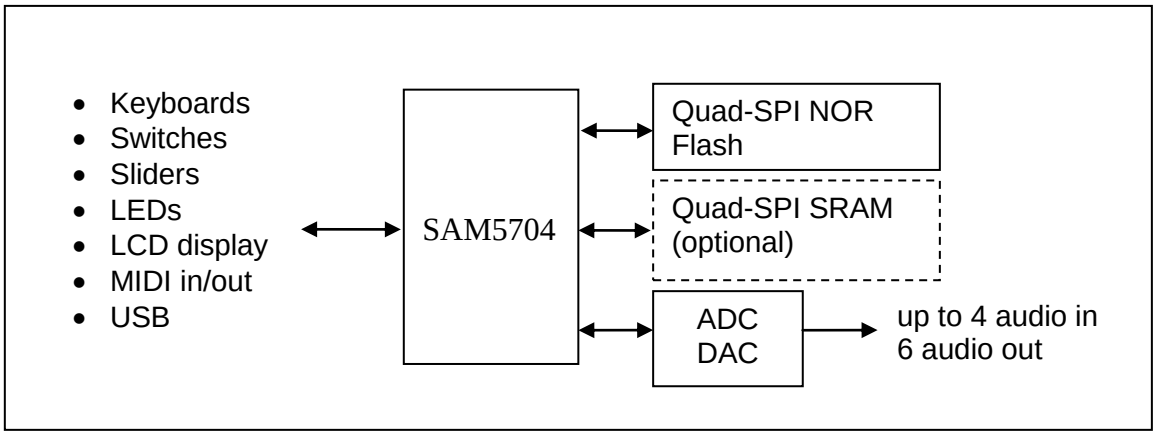
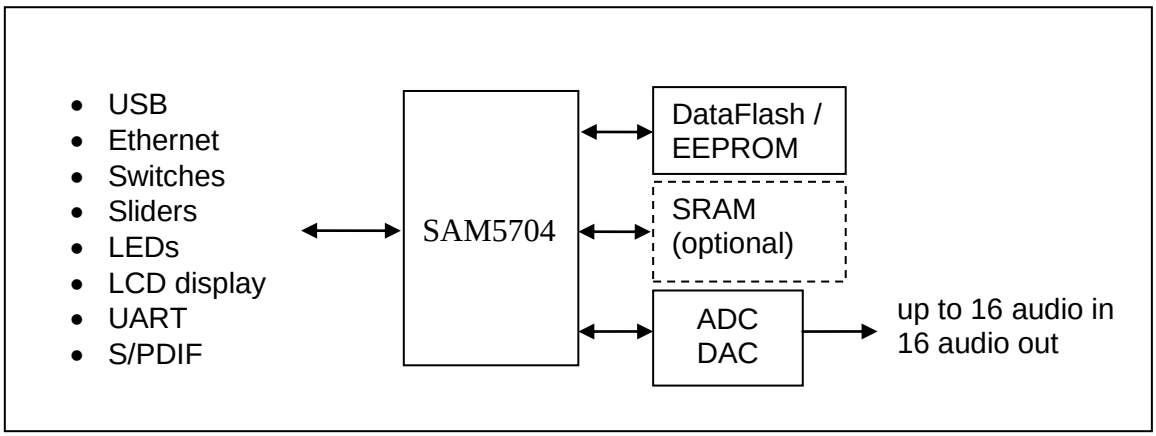
2. Typical application examples

2.1. **Low-Cost Piano / Keyboard** (using Memory Configuration 6)



- 81 voice high quality sound synthesis (polynomial interpolation, new filter modes…) with sound banks in Quad-SPI-NOR, “Octal-SPI” with 2 Quad-SPI devices
- Copy protected sound banks in cost saving memories (Quad-SPI-NOR)
- High quality effects (Reverb, Chorus, Equalizer)
- Direct connection to keyboard, switches, LEDs, LCD
- 10-bit ADC for sliders and pedals
- USB-MIDI or USB-Disk

2.2. **Low-Cost Professional Audio Applications** (using Memory Configuration 5)



- USB 2.0 High Speed port e.g. for AudioClass 2.0 compliant USB Audio interface with up to 16 Audio IN and 16 Audio OUT channels at up to 192KHz sampling rate / 24bit
- 10/100 Mbps Ethernet MAC with RMII interface to external PHY
- Up to 192kHz S/PDIF interface (IEC60958) with clock recovery (concurrent IN/OUT)
- On-die synchronization PWM mechanism controlling external VCXO for audio streaming from external sources
- Vast library of ready to use high-class filters, dynamic processing, delays, effects of all kind…
- Typical applications: Speaker processing, USB Audio interfaces, Effect units etc.

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3. SAM5704B capacity and I/O configuration

The SAM5704B can run a firmware from an external NOR Flash, Quad-SPI NOR Flash, NAND Flash or DataFlash/EEPROM memory, by using Cache mode or boot-load mechanism. A firmware can also be down-loaded from a Host CPU, and SAM5704B runs the firmware from local RAM. The SAM5704B can use its local RAM for effects processing (the embedded RAM is widely configurable for best choice between program and effects memory space), it can be extended by external low cost SRAM, Quad-SPI RAM or SDRAM. The SAM5704B is the ideal choice for low cost digital pianos and keyboards, and also professional audio products like Mixer effect devices, Speaker processing, USB-Audio Interfaces etc., with low count of required external components and many configurable I/Os.

3.1. DSP considerations

The SAM5704B includes 4 x P24XT DSPs.
The table below lists the performance achievable by the P24:

Function	P24XTs required
81-voice Wavetable Synthesis @48kHz	3
stereo Reverb, Chorus, Equalizer and Keyboard Scanning @48kHz	1
56 double precision filters bands @48kHz	1
8 in / 8 out USB Audio Interface @48KHz	1

3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pin-out to identify the exclusions). The two main types of operation are host controlled and stand-alone.

3.2.1. Host-controlled operation

There are 3 main ways of communication with a host processor:

- 8-bit parallel bi-directional Host interface
  signals: D7-D0, CS/, WR/, RD/, A0, IRQ
- Asynchronous serial (UART), 2x MIDI_IN and 2x MIDI_OUT
- Synchronous serial
  signals: SSDIN, SSCLK, SSYNC, SSINT/

3.2.2. Stand-alone operation

Possible stand-alone modes are:
- Firmware into external parallel NOR Flash
- Firmware into external NAND Flash memory
- Firmware into external SPI NOR Flash connected on Multi-Purpose Quad SPI bus
- Firmware into external SPI NOR Flash connected on Quad SPI NOR Flash bus
- Firmware into external SPI NOR Flash connected on Quad SPI SRAM bus

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4. SAM5704B PINOUT

4.1. Memory Config

The SAM5704B can be used in 6 different hardware configurations called Memory Config. This flexible architecture allows selecting the appropriate memory interfaces for each application.

Memory Config can be defined in two ways:
1. Sensed at start-up: Memory Config is defined by the level on MC0, MC1 and MC2 pins sensed at start-up. MC0 sensed on CKOUT, MC1 sensed on SPICK and MC2 sensed on MIDI_OUT.
2. Read from Efuse MC bits: Memory Config is preprogrammed in embedded eFuse. In this case MC0-MC2 pins will not be sensed.

4.1.1. Memory Config Table

MC2	MC1	MC0	Memory Config	Description
0	0	0	1	SDRAM + NOR Flash.
0	0	1	2	SRAM + NOR Flash.
0	1	0	3	SDRAM + NAND Flash.
0	1	1	4	SRAM + NAND Flash.
1	0	0	5	SRAM + Ethernet.
1	0	1	6	Quad NOR Flash + Quad SRAM + Ethernet + Versatile IOs (Keyboard applications)
1	1	0	-	Reserved for test. Do not use
1	1	1	-	Reserved for test. Do not use

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4.2. Pin-out by pin

4.2.1. Memory Config 1: SDRAM + NOR Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	DABD0
3	STIN	35	MD4	67	AGND	99	DAAD0
4	STOUT	36	MD5	68	DAAD1	100	CS/
5	MIDI_IN1	37	MD6	69	DABD1	101	RD/
6	MIDI_OUT1	38	MD7	70	DAAD2	102	WR/
7	SPICK	39	MD8	71	MA16	103	IRQ
8	SPICS0/	40	MD9	72	MA17	104	A0
9	VD33	41	VD33	73	MA18	105	VD33
10	NRCS0/	42	MD10	74	MWE/	106	SPI0
11	NRCS1/	43	MD11	75	MOE/	107	SPI1
12	VD33	44	MD12	76	MA19	108	SPI2
13	DRCAS/	45	MD13	77	VD33	109	SPI3
14	DRRAS/	46	MD14	78	MA20	110	VD12
15	DRWE/	47	MD15	79	MA21	111	D0
16	DRCKE	48	VD33	80	MA22	112	D1
17	DRCS0/	49	MA4	81	MA23	113	D2
18	DRCS1/	50	MA5	82	MA24	114	D3
19	VD33	51	MA6	83	MA25	115	D4
20	MA0	52	MA7	84	MA26	116	D5
21	MA1	53	MA8	85	VD12	117	D6
22	MA2	54	MA9	86	VD33	118	D7
23	MA3	55	VD12	87	USBID	119	VD33
24	VD12	56	MA10	88	FSOURCE	120	VD33O
25	DRDM0	57	MA11	89	OSC1_X1	121	OSC2_X1
26	DRDM1	58	MA12	90	OSC1_X2	122	OSC2_X2
27	VD33	59	MA13	91	VD33U	123	GNDO
28	DRCK	60	MA14	92	USBDM	124	GND
29	MD0	61	MA15	93	USBDP	125	VC12
30	MD1	62	VD33	94	GNDU	126	OUTVC12
31	MD2	63	CLBD	95	USBREF	127	VD33R
32	MD3	64	WSBD	96	GND	128	GNDR

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4.2.2. Memory Config 2: SRAM + NOR Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	DABD0
3	STIN	35	MD4	67	AGND	99	DAAD0
4	STOUT	36	MD5	68	DAAD3	100	DAAD5
5	MIDI_IN1	37	MD6	69	SRCS/	101	DABD4
6	MIDI_OUT1	38	MD7	70	DAAD2	102	DABD5
7	SPICK	39	MD8	71	MA16	103	DAAD4
8	SPICS0/	40	MD9	72	MA17	104	DABD6
9	VD33	41	VD33	73	MA18	105	VD33
10	NRCS0/	42	MD10	74	MWE/	106	SPI0
11	NRCS1/	43	MD11	75	MOE/	107	SPI1
12	VD33	44	MD12	76	MA19	108	SPI2
13	CS/	45	MD13	77	VD33	109	SPI3
14	RD/	46	MD14	78	MA20	110	VD12
15	WR/	47	MD15	79	MA21	111	D0
16	IRQ	48	VD33	80	MA22	112	D1
17	DABD3	49	MA4	81	MA23	113	D2
18	DAAD1	50	MA5	82	MA24	114	D3
19	VD33	51	MA6	83	MA25	115	D4
20	MA0	52	MA7	84	MA26	116	D5
21	MA1	53	MA8	85	VD12	117	D6
22	MA2	54	MA9	86	VD33	118	D7
23	MA3	55	VD12	87	USBID	119	VD33
24	VD12	56	MA10	88	FSOURCE	120	VD33O
25	A0	57	MA11	89	OSC1_X1	121	OSC2_X1
26	DABD1	58	MA12	90	OSC1_X2	122	OSC2_X2
27	VD33	59	MA13	91	VD33U	123	GNDO
28	DABD2	60	MA14	92	USBDM	124	GND
29	MD0	61	MA15	93	USBDP	125	VC12
30	MD1	62	VD33	94	GNDU	126	OUTVC12
31	MD2	63	CLBD	95	USBREF	127	VD33R
32	MD3	64	WSBD	96	GND	128	GNDR

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4.2.3. Memory Config 3: SDRAM + NAND Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	NDCE0/
3	STIN	35	MD4	67	AGND	99	NDCE1/
4	STOUT	36	MD5	68	DAAD1	100	NDR|B/
5	MIDI_IN1	37	MD6	69	DABD1	101	NDALE
6	MIDI_OUT1	38	MD7	70	DAAD2	102	NDCLE
7	SPICK	39	MD8	71	CS/	103	NDWE/
8	SPICS0/	40	MD9	72	RD/	104	NDRE/
9	VD33	41	VD33	73	WR/	105	VD33
10	DAAD0	42	MD10	74	IRQ	106	SPI0
11	DABD0	43	MD11	75	A0	107	SPI1
12	VD33	44	MD12	76	D0	108	SPI2
13	DRCAS/	45	MD13	77	VD33	109	SPI3
14	DRRAS/	46	MD14	78	D1	110	VD12
15	DRWE/	47	MD15	79	D2	111	NDIO0
16	DRCKE	48	VD33	80	D3	112	NDIO1
17	DRCS0/	49	MA4	81	D4	113	NDIO2
18	DRCS1/	50	MA5	82	D5	114	NDIO3
19	VD33	51	MA6	83	D6	115	NDIO4
20	MA0	52	MA7	84	D7	116	NDIO5
21	MA1	53	MA8	85	VD12	117	NDIO6
22	MA2	54	MA9	86	VD33	118	NDIO7
23	MA3	55	VD12	87	USBID	119	VD33
24	VD12	56	MA10	88	FSOURCE	120	VD33O
25	DRDM0	57	MA11	89	OSC1_X1	121	OSC2_X1
26	DRDM1	58	MA12	90	OSC1_X2	122	OSC2_X2
27	VD33	59	MA13	91	VD33U	123	GNDO
28	DRCK	60	MA14	92	USBDM	124	GND
29	MD0	61	MA15	93	USBDP	125	VC12
30	MD1	62	VD33	94	GNDU0	126	OUTVC12
31	MD2	63	CLBD	95	USBREF	127	VD33R
32	MD3	64	WSBD	96	GND	128	GNDR

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4.2.4. Memory Config 4: SRAM + NAND Flash

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	NDCE0/
3	STIN	35	MD4	67	AGND	99	NDCE1/
4	STOUT	36	MD5	68	DAAD3	100	NDR|B/
5	MIDI_IN1	37	MD6	69	SRCS/	101	NDALE
6	MIDI_OUT1	38	MD7	70	DAAD2	102	NDCLE
7	SPICK	39	MD8	71	MA16	103	NDWE/
8	SPICS0/	40	MD9	72	MA17	104	NDRE/
9	VD33	41	VD33	73	MA18	105	VD33
10	DAAD0	42	MD10	74	MWE/	106	SPI0
11	DABD0	43	MD11	75	MOE/	107	SPI1
12	VD33	44	MD12	76	D0	108	SPI2
13	CS/	45	MD13	77	VD33	109	SPI3
14	RD/	46	MD14	78	D1	110	VD12
15	WR/	47	MD15	79	D2	111	NDIO0
16	IRQ	48	VD33	80	D3	112	NDIO1
17	DABD3	49	MA4	81	D4	113	NDIO2
18	DAAD1	50	MA5	82	D5	114	NDIO3
19	VD33	51	MA6	83	D6	115	NDIO4
20	MA0	52	MA7	84	D7	116	NDIO5
21	MA1	53	MA8	85	VD12	117	NDIO6
22	MA2	54	MA9	86	VD33	118	NDIO7
23	MA3	55	VD12	87	USBID	119	VD33
24	VD12	56	MA10	88	FSOURCE	120	VD33O
25	A0	57	MA11	89	OSC1_X1	121	OSC2_X1
26	DABD1	58	MA12	90	OSC1_X2	122	OSC2_X2
27	VD33	59	MA13	91	VD33U	123	GNDO
28	DABD2	60	MA14	92	USBDM	124	GND
29	MD0	61	MA15	93	USBDP	125	VC12
30	MD1	62	VD33	94	GNDU	126	OUTVC12
31	MD2	63	CLBD	95	USBREF	127	VD33R
32	MD3	64	WSBD	96	GND	128	GNDR

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4.2.5. Memory Config 5: SRAM + Ethernet

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	DABD3
3	STIN	35	MD4	67	AGND	99	DAAD2
4	STOUT	36	MD5	68	DAAD1	100	DAAD5
5	MIDI_IN1	37	MD6	69	SRCS/	101	DABD4
6	MIDI_OUT1	38	MD7	70	REF_CLK	102	DABD5
7	SPICK	39	MD8	71	MA16	103	DAAD4
8	SPICS0/	40	MD9	72	MA17	104	DAAD3
9	VD33	41	VD33	73	MA18	105	VD33
10	DAAD0	42	MD10	74	MWE/	106	SPI0
11	DABD0	43	MD11	75	MOE/	107	SPI1
12	VD33	44	MD12	76	TXD0	108	SPI2
13	CS/	45	MD13	77	VD33	109	SPI3
14	RD/	46	MD14	78	TXD1	110	VD12
15	WR/	47	MD15	79	RXD0	111	D0
16	IRQ	48	VD33	80	RXD1	112	D1
17	MDC	49	MA4	81	TX_EN	113	D2
18	MDIO	50	MA5	82	CRS_DV	114	D3
19	VD33	51	MA6	83	RX_ER	115	D4
20	MA0	52	MA7	84	ETH_RES/	116	D5
21	MA1	53	MA8	85	VD12	117	D6
22	MA2	54	MA9	86	VD33	118	D7
23	MA3	55	VD12	87	USBID	119	VD33
24	VD12	56	MA10	88	FSOURCE	120	VD33O
25	A0	57	MA11	89	OSC1_X1	121	OSC2_X1
26	DABD1	58	MA12	90	OSC1_X2	122	OSC2_X2
27	VD33	59	MA13	91	VD33U	123	GNDO
28	DABD2	60	MA14	92	USBDM	124	GND
29	MD0	61	MA15	93	USBDP	125	VC12
30	MD1	62	VD33	94	GNDU	126	OUTVC12
31	MD2	63	CLBD	95	USBREF	127	VD33R
32	MD3	64	WSBD	96	GND	128	GNDR

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4.2.6. Memory Config 6: Quad NOR Flash + Quad SRAM.+ Ethernet + Versatile IOs (Keyboard application)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	RST/	33	GND	65	VIN	97	CKOUT
2	TEST	34	VD33	66	VA33	98	DABD0
3	STIN	35	QNR4	67	AGND	99	DAAD0
4	STOUT	36	QNR5	68	SEL0	100	ROW0
5	MIDI_IN1	37	QNR6	69	DABD1	101	ROW1
6	MIDI_OUT1	38	QNR7	70	REF_CLK	102	ROW2
7	SPICK	39	QSR0	71	MK8	103	ROW3
8	SPICS0/	40	QSR1	72	MK9	104	QNRCK
9	VD33	41	VD33	73	MK10	105	VD33
10	QSRCS/	42	QSR2	74	QSRCK	106	BR0
11	QNRCS0/	43	QSR3	75	SEL1	107	BR1
12	VD33	44	SPI0	76	MK0	108	BR2
13	CS/	45	SPI1	77	VD33	109	BR3
14	RD/	46	SPI2	78	MK1	110	VD12
15	WR/	47	SPI3	79	MK2	111	BR4
16	IRQ	48	VD33	80	MK3	112	BR5
17	MDC	49	D4	81	MK4	113	BR6
18	MDIO	50	D5	82	MK5	114	BR7
19	VD33	51	D6	83	MK6	115	BR8
20	D0	52	D7	84	MK7	116	BR9
21	D1	53	TXD0	85	VD12	117	BR10
22	D2	54	TXD1	86	VD33	118	QNRCS1/
23	D3	55	VD12	87	USBID	119	VD33
24	VD12	56	RXD0	88	FSOURCE	120	VD33O
25	A0	57	RXD1	89	OSC1_X1	121	OSC2_X1
26	DAAD1	58	TX_EN	90	OSC1_X2	122	OSC2_X2
27	VD33	59	CRS_DV	91	VD33U	123	GNDO
28	DABD2	60	RX_ER	92	USBDM	124	GND
29	QNR0	61	ETH_RES/	93	USBDP	125	VC12
30	QNR1	62	VD33	94	GNDU	126	OUTVC12
31	QNR2	63	CLBD	95	USBREF	127	VD33R
32	QNR3	64	WSBD	96	GND	128	GNDR

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4.3. Pin description

White cells describes Primary function of the pin
Grey cells describes Secondary function of the pin
Pink cells describes GPIO function of the pin
Yellow cells describes special function of the pin at start-up

PD indicates pin with built-in pull-down resistor. (PD) indicates that the pull-down can be disabled.
PU indicates pin with built-in pull-up resistor. (PU) indicates that the pull-down can be disabled.
5VT indicates a 5 volt tolerant Input or I/O pin.
DR4, DR8, DR12 indicates driving capability at VOL, VOH (see § 7.3.- D.C. Characteristics)
SR3: If GPIO is used as input, an external 330Ω (min) serial resistor is needed for safe ROM boot.
SR7: If GPIO is used as input, an external 750Ω (min) serial resistor is needed for safe ROM boot.

4.3.1. Power Supply Group

Pin name	Pin#	Type	Mem Cfg	Description
VD12	24,55, 85,110	PWR	1-6	Power for the internal core, +1.2V nominal (1.2V ± 10 %). These pins must be connected to the output of the regulator OUTVC12 (pin 214). 100nF+10nF capacitors should be connected between each of these pins and a close ground plane. 10µF should be added on two opposite sides.
VC12	125	PWR	1-6	Power for the internal PLL, +1.2V nominal (1.2V ± 10 %). This pin must be connected to the output of the regulator OUTVC12 (pin 126). 10µF+100nF capacitors should be connected between this pin and a close ground plane.
VD33	9,12,19, 27,34, 41,48, 62,77, 86,105, 119,	PWR	1-6	+3.3V power for periphery. All these pins should be returned to nominal 3.3V. 100nF capacitors should be connected between half of these pins and a close ground plane. 10µF should be added on two opposite sides.
GND	33,96, 124	PWR	1-6	Digital ground. All these pins should be returned to ground plane
VD33O	120	PWR	1-6	+3.3V power for internal oscillator. A 100nF filtering capacitor should be connected between VD33O and GNDO.
GNDO	123	PWR	1-6	Digital ground for internal oscillator OSC2. This pin should be returned to the ground plane
VD33R	127	PWR	1-6	+3.3V power for internal 3.3V to 1.2 V regulator OSC2. A 10µF filtering capacitor should be connected between VD33R and GNDR.
GNDR	128	PWR	1-6	Digital ground for internal 3.3V to 1.2 V regulator. This pin should be returned to the ground plane
VD33U	91	PWR	1-6	+3.3V power for internal USB port. 10µF+100nF+10nF capacitors should be connected between VD33U and GNDU.
GNDU	94	PWR	1-6	Digital ground for internal USB port. This pin should be returned to a ground plane

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Pin name	Pin#	Type	Mem Cfg	Description
VA33	66	PWR	1-6	Analog power for the ADC. Should be connected to a clean analog +3.3V nominal. 10µF+100nF capacitors should be connected between VA33 and AGND.
AGND	67	PWR	1-6	Analog ground for ADC. Should be returned to a clean analog ground plane.
OUTVC12	126	PWR	1-6	3.3V to 1.2 V regulators output. The built-in regulator gives 1.2V for internal use. VC12 and VD12 pins should also be connected to this pin. Decoupling capacitors 3.3µF+100nF or 4.7µF+100nF must be connected between OUTVC12 pin and GNDR
FSOURCE	88	PWR	1-6	Fuse Program source input. - Left open or grounded (recommended) for normal operation. - Connected to +3.3V/12mA(min) power supply for fuse programming. 10µF+100nF capacitors should be connected between FSOURCE and ground plane.

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4.3.2. Test, Reset, Oscillators, USB, ADC, MIDI / UART, Debug

Pin name	Pin#	Type	Mem Cfg	Description
TEST	2	In PD	1-6	Test input. Should be grounded or left open.
RST/	1	In	1-6	Master reset and Power down. Schmitt trigger input. RST/ should be held low during at least 10ms after power is applied. On the rising edge of RST/ the chip enters its initialization routine.
OSC1_X1-OSC1_X2	89,90	-	1-6	Main Oscillator OSC1 - Dual crystal design: 12 MHz external crystal connection for USB embedded Ports and Ethernet controller. - Single crystal design: USB, Ethernet, System and audio clocks are derived fromOSC1. Crystal value can be: ° 12MHz if USB or Ethernet in use. ° 11.2896MHz or 12.288MHz if USB is not used - An external clock can be connected to OSC1_X1.
OSC2_X1-OSC2_X2	121,122	-	1-6	- Dual crystal design: System and audio clocks are derived from OSC2_X1-OSC2_X2. Crystal value can be 11.2896MHz or 12.288MHz. - Single crystal design: These pins should be left unconnected. - An external clock can be connected to OSC2_X1. (e.g., enslavement to external VCX0 driven by SAM5704B PWM generator)
USBDM	92	I/O	1-6	USB D- connection (analog) of USB Port
USBDP	93	I/O	1-6	USB D+ connection (analog) of USB Port
USBREF	95	In	1-6	A 12kΩ ± 1% resistor should be connected between this pin and GNDU. Unconnected if USB Port is not used.
USBID	87	In 5VT	1-6	USB ID. Detect if A device or B device in case of USB Port running in Dual Role mode.
MIDI_OUT2	87	Out DR4	1-6	Additional Serial MIDI Out (UART Tx)
P8.15	87	I/O 5VT DR4	1-6	General purpose I/O pin.
VIN	65	In	1-6	Analog input of embedded ADC: Multiple sliders should be connected through external analog multiplexer like 4051. Channels should be selected by ROW0-ROW3 if available, or GPIOs.
MIDI_IN1	5	In 5VT (PU)	1-6	Serial MIDI In (UART Rx)
MIDI_IN2	5	In 5VT (PU)	1-6	Additional Serial MIDI In (UART Rx)
P0.14	5	I/O 5VT (PU) DR4	1-6	General purpose I/O pin.
MIDI_OUT1	6	Out DR4	1-6	Serial MIDI Out (UART Tx)
P0.9	6	I/O DR4	1-6	General purpose I/O pin.
MC2	6	In	1-6	Memory Config 2. This pin is sensed at power up. MC2|MC1|MC0 setting allows boot ROM code to start the right Memory Config.
STIN	3	In PD	1-6	Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. It should be grounded or left open for normal operation.
STOUT	4	Out DR4	1-6	Serial test output. 57.6 kbauds async output used for firmware debugging.
MIDI_IN2	4	In 5VT (PU)	1-6	Additional Serial MIDI In (UART Rx)
P0.15	4	I/O 5VT (PU) DR4	1-6	General purpose I/O pin.

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4.3.3. Multi-purpose Quad SPI as primary function

Pin name	Pin#	Type	Mem Cfg	Description
SPICK	7	Out DR8	1-6	Data clock for Multi-purpose Quad SPI interface.
PWM_OUT	7	Out DR8	1-6	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.14	7	I/O 5VT DR8 SR3	1-6	General purpose I/O pin.
MC1	7	In	1-6	Memory Config 1. This pin is sensed at power-up. MC2|MC1|MC0 setting allows boot ROM code to start the right Memory Config.
SPICS0/	8	Out DR8	1-6	Chip select 0 for Multi-purpose Quad SPI interface.
P7.15	8	I/O 5VT (PU) DR8 SR3	1-6	General purpose I/O pin.
SPI0	106	I/O 5VT DR12	1-5	SPI data 0. - Serial Output to SI peripheral Input for Single bit data commands (MOSI). - Serial IO0 for Quad commands.
SPDIF_OI	106	I/O 5VT DR12	1-5	SPDIF Output or Input. Output by default.
P7.10	106	I/O.5VT DR12 SR3	1-5	General purpose I/O pin.
SPI1	107	I/O 5VT DR12	1-5	SPI data 1. - Serial Input from SO peripheral Output for Single bit data commands (MISO). - Serial IO1 for Quad commands.
SPDIF_IO	107	I/O 5VT DR12	1-5	SPDIF Input or Output. Input by default.
P7.11	107	I/O.5VT DR12	1-5	General purpose I/O pin.
SPI2	108	I/O 5VT (PU) DR12	1-5	SPI data 2. Serial IO2 Quad commands
PWM_OUT	108	Out DR12	1-5	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.12	108	I/O.5VT (PU) DR12	1-5	General purpose I/O pin.
SPI3	109	I/O 5VT (PU) DR12	1-5	SPI data 2. Serial IO2 Quad commands
SPDIF_IO	109	I/O.5VT (PU) DR12	1-5	SPDIF Input or Output. Input by default.
P7.13	109	I/O.5VT (PU) DR12	1-5	General purpose I/O pin.
SPI0	44	I/O 5VT DR12	6	SPI data 0. - Serial Output to SI peripheral Input for Single bit data commands. - Serial IO0 for Quad commands.
SPDIF_OI	44	I/O 5VT DR12	6	SPDIF Output or Input. Output by default.
P7.10	44	I/O 5VT DR12	6	General purpose I/O pin.
SPI1	45	I/O 5VT DR12	6	SPI data 1. - Serial Input from SO peripheral Output for Single bit data commands. - Serial IO1 for Quad commands.
SPDIF_IO	45	I/O 5VT DR12	6	SPDIF Input or Output. Input by default.
P7.11	45	I/O 5VT DR12	6	General purpose I/O pin.
SPI2	46	I/O 5VT (PU) DR12	6	SPI data 2. Serial IO2 Quad commands External 100k pull-up resistor is needed for safe ROM boot.
PWM_OUT	46	Out DR12	6	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio.
P7.12	46	I/O 5VT (PU) DR12	6	General purpose I/O pin.
SPI3	47	I/O 5VT (PU) DR12	6	SPI data 2. Serial IO2 Quad commands External 100k pull-up resistor is needed for safe ROM boot.
SPDIF_IO	47	I/O. 5VT (PU) DR12	6	SPDIF Input or Output. Input by default.
P7.13	47	I/O. 5VT (PU) DR12	6	General purpose I/O pin.

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4.3.4. Ethernet as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MDC	17	Out DR12	5,6	Management Interface (MII) Clock to the Ethernet PHY.
XWSBD0	17	In 5VT	5,6	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
P8.9	17	I/O 5VT DR12	5,6	General purpose I/O pin.
MDIO	18	I/O 5VT DR12	5,6	Management Interface (MII) Data I/O to the Ethernet PHY.
XCLBD0	18	In 5VT	5,6	External clock bit 0 for digital audio inputs DAAD[7:0].
P8.10	18	I/O 5VT DR12	5,6	General purpose I/O pin.
REF_CLK	70	Out DR8	5,6	25MHz RMII reference clock to the Ethernet PHY.
SPICS1/	70	Out DR8	5,6	Chip select 1 for Multi-purpose Quad SPI interface.
P8.0	70	I/O (PU) 5VT DR8	5,6	General purpose I/O pin.
ETH_RES/	84	Out DR8	5	Reset output to the Ethernet PHY
XWSBD1	84	In. 5VT	5	External word select clock 1 for digital audio inputs DAAD[7:0].
P8.1	84	I/O 5VT DR8	5	General purpose I/O pin.
RX_ER	83	In 5VT	5	RMII Receive Error from the Ethernet PHY.
XCLBD1	83	In 5VT	5	External clock bit 1 for digital audio inputs DAAD[7:0].
P8.2_IntB	83	I/O 5VT DR8	5	General purpose I/O pin. External Interrupt source IntB.
RXD0	79	In 5VT	5	RMII Receive Data 0 from the Ethernet PHY.
DAAD6	79	In 5VT	5	Stereo audio digital input 6, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.3	79	I/O 5VT DR8	5	General purpose I/O pin.
RXD1	80	In 5VT	5	RMII Receive Data 1 from the Ethernet PHY.
DAAD7	80	In 5VT	5	Stereo audio digital input 7, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.4	80	I/O DR8 5VT	5	General purpose I/O pin.
CRS_DV	82	In 5VT	5	RMII Carrier Sense/Receive Data Valid from the Ethernet PHY
DABD6	82	Out DR8	5	Stereo audio digital output 6, I2S or MSB format.
P8.5	82	I/O 5VT DR8	5	General purpose I/O pin.
TXD0	76	Out DR8	5	RMII Transmit Data 0 to the Ethernet PHY.
DABD7	76	Out DR8	5	Stereo audio digital output 7, I2S or MSB format.
P8.6	76	I/O 5VT DR8	5	General purpose I/O pin.
TXD1	78	Out DR8	5	RMII Transmit Data 1 to the Ethernet PHY.
SPICS2/	78	Out DR8	5	Chip select 2 for Multi-purpose Quad SPI interface.
P8.7	78	I/O 5VT (PU) DR8	5	General purpose I/O pin.
TX_EN	81	Out DR8	5	RMII Transmit Enable to the Ethernet PHY.
SPICS3/	81	Out DR8	5	Chip select 3 for Multi-purpose Quad SPI interface.
P8.8	81	I/O 5VT (PU) DR8	5	General purpose I/O pin.
ETH_RES/	61	Out DR12	6	Reset output to the Ethernet PHY
XWSBD1	61	In 5VT	6	External word select clock 1 for digital audio inputs DAAD[7:0].
P8.1	61	I/O 5VT DR12	6	General purpose I/O pin.

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Pin name	Pin#	Type	Mem Cfg	Description
RX_ER	60	In 5VT	6	RMII Receive Error Output from the Ethernet PHY.
XCLBD1	60	In 5VT2	6	Optional clock bit for digital audio inputs DAAD[7:0]. Used for sampling rate conversion, for external incoming digital audio.
P8.2_IntB	60	I/O 5VT DR12	6	General purpose I/O pin. External Interrupt source IntB.
RXD0	56	In 5VT	6	RMII Receive Data Output 0 from the Ethernet PHY.
DAAD6	56	In 5VT	6	Stereo audio digital input 6, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.3	56	I/O 5VT DR12	6	General purpose I/O pin.
RXD1	57	In 5VT	6	RMII Receive Data Output 1 from the Ethernet PHY.
DAAD7	57	In 5VT	6	Stereo audio digital input 7, I2S or MSB format. Can operate on CLBD master rate or XCLBD external rate.
P8.4	57	I/O 5VT DR12	6	General purpose I/O pin.
CRS_DV	59	In 5VT	6	RMII Carrier Sense/Receive Data Valid Output from the Ethernet PHY
DABD6	59	Out DR12	6	Stereo audio digital output 6, I2S or MSB format.
P8.5	59	I/O 5VT DR12	6	General purpose I/O pin.
TXD0	53	Out DR12	6	RMII Transmit Data 0 to the Ethernet PHY.
DABD7	53	Out DR12[2]	6	Stereo audio digital output 7, I2S or MSB format.
P8.6	53	I/O 5VT DR12	6	General purpose I/O pin.
TXD1	54	Out DR12	6	RMII Transmit Data 1 to the Ethernet PHY.
SPICS2/	54	Out DR12	6	Chip select 2 for Multi-purpose Quad SPI interface. Need external 100k pull-up resistor if firmware is in device selected by SPICS0/.
P8.7	54	I/O 5VT DR12	6	General purpose I/O pin.
TX_EN	58	Out DR12	6	RMII Transmit Enable to the Ethernet PHY.
SPICS3/	58	Out DR12	6	Chip select 3 for Multi-purpose Quad SPI interface. Need external 100k pull-up resistor if firmware is in device selected by SPICS0/.
P8.8	58	I/O 5VT DR12	6	General purpose I/O pin.

4.3.5. Host Parallel Interface as primary function

Pin name	Pin#	Type	Mem Cfg	Description
D0-D7	111-118	I/O 5VT DR8	1,2,5	Host parallel interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0-A1 address input.
DAAD2	111	In 5VT	1,2,5	Stereo audio digital input 2, I2S or MSB format.
DABD4	112	Out DR8	1,2,5	Stereo audio digital output 4, I2S or MSB format.
DABD3	113	Out DR8	1,2,5	Stereo audio digital output 3, I2S or MSB format.
DABD2	114	Out DR8	1,2,5	Stereo audio digital output 2, I2S or MSB format.
XWSBD1	115	In 5VT	1,2,5	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD1	116	In 5VT	1,2,5	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD0	117	In 5VT	1,2,5	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
XCLBD0	118	In 5VT	1,2,5	External clock bit for digital audio inputs DAAD[7:0].
P0.0-P0.7	111-118	I/O 5VT DR8	1,2,5	General purpose I/O pins. Can be individually programmed as input or output.

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Pin name	Pin#	Type	Mem Cfg	Description
D0-D7	76 78-84	I/O 5VT DR8	3,4	Host parallel interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0-A1 address input.
DAAD2	76	In 5VT	3,4	Stereo audio digital input 2, I2S or MSB format.
DABD4	78	Out DR8	3,4	Stereo audio digital output 4, I2S or MSB format.
DABD3	79	Out DR8	3,4	Stereo audio digital output 3, I2S or MSB format.
DABD2	80	Out DR8	3,4	Stereo audio digital output 2, I2S or MSB format.
XWSBD1	81	In 5VT	3,4	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD1	82	In 5VT	3,4	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD0	83	In 5VT	3,4	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
XCLBD0	84	In 5VT	3,4	External clock bit for digital audio inputs DAAD[7:0].
P0.0-P0.7	76, 78-84	I/O 5VT DR8	3,4	General purpose I/O pins. Can be individually programmed as input or output.
D0-D7	20-23 49-52	I/O 5VT DR12	6	Host parallel interface data. Output if CS/ and RD/ are low (read from chip), input if CS/ and WR/ are low (write to chip). Type of data defined by A0-A1 address input.
DAAD2	20	In 5VT	6	Stereo audio digital input 2, I2S or MSB format.
DABD4	21	Out DR12	6	Stereo audio digital output 4, I2S or MSB format.
DABD3	22	Out DR12	6	Stereo audio digital output 3, I2S or MSB format.
DABD2	23	Out DR12	6	Stereo audio digital output 2, I2S or MSB format.
XWSBD1	49	In 5VT	6	Optional word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD1	50	In 5VT	6	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD0	51	In 5VT	6	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
XCLBD0	52	In 5VT	6	External clock bit 0 for digital audio inputs DAAD[7:0].
P0.0-P0.7	20-23, 49,52	I/O 5VT DR12	6	General purpose I/O pins. Can be individually programmed as input or output.
IRQ	103	Out DR8	1	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	103	Out DR8	1	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8_IntA	103	I/O 5VT DR8	1	General purpose I/O pin. External Interrupt source IntA.
A0	104	In 5VT	1	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	104	In 5VT	1	Serial Slave Synchronous Interface clock input.
P0.10	104	I/O 5VT DR8	1	General purpose I/O pin.
CS/	100	In 5VT	1	Host parallel interface chip select, active low.
SSYNC	100	In 5VT	1	Serial Slave Synchronous Interface input sync signal.
P0.11	100	I/O 5VT DR8	1	General purpose I/O pin.

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Pin name	Pin#	Type	Mem Cfg	Description
WR/	102	In 5VT	1	Host parallel interface write, active low. D7-D0 or D15-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	102	In 5VT	1	Serial Slave Synchronous Interface input data.
P0.12	102	I/O 5VT DR8	1	General purpose I/O pin.
RD/	101	In 5VT	1	Host parallel interface read, active low. D7-D0 or D15-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	101	Out 5VT	1	Additional Serial MIDI Out (UART Tx) **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	101	I/O 5VT DR8	1	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot. If used as input, should not be driven low by external device while ROM boot.**
IRQ	16	Out DR12	2,4-6	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	16	Out DR12	2,4-6	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8_IntA	16	I/O 5VT DR12	2,4-6	General purpose I/O pin. External Interrupt source IntA.
A0	25	In 5VT	2,4-6	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	25	In 5VT	2,4-6	Serial Slave Synchronous Interface clock input.
P0.10	25	I/O 5VT DR12	2,4-6	General purpose I/O pin.
CS/	13	In 5VT	2,4-6	Host parallel interface chip select, active low.
SSYNC	13	In 5VT	2,4-6	Serial Slave Synchronous Interface input sync signal.
P0.11	13	I/O 5VT DR12	2,4-6	General purpose I/O pin.
WR/	15	In 5VT	2,4-6	Host parallel interface write, active low. D7-D0 or D15-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	15	In 5VT	2,4-6	Serial Slave Synchronous Interface input data.
P0.12	15	I/O 5VT DR12	2,4-6	General purpose I/O pin.
RD/	14	In 5VT	2,4-6	Host parallel interface read, active low. D7-D0 or D15-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	14	Out DR12	2,4-6	Additional Serial MIDI Out. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	14	I/O 5VT DR12	2,4-6	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot. If used as input, should not be driven low by external device while ROM boot.**

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Pin name	Pin#	Type	Mem Cfg	Description
IRQ	74	Out DR8	3	Host parallel interface mode 0 interrupt request. High when data is ready to be transferred from chip to host. Reset by a read from host (CS/=0 and RD/=0). **External 100k max pull-down resistor is needed for safe ROM boot.**
SSINT/	74	Out DR8	3	Serial Slave Synchronous Interface data request, active low. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.8_IntA	74	I/O 5VT DR8	3	General purpose I/O pin. External Interrupt source IntA.
A0	75	In 5VT	3	Host parallel interface address 0. In case A1=0 (mode 0): Indicates data/status or data/ctrl transfer type (CS/ RD/ low or CS/ WR/ low). In case A1=1 (mode 1): the A0 input is “don’t care”.
SSCLK	75	In 5VT	3	Serial Slave Synchronous Interface clock input.
P0.10	75	I/O 5VT DR8	3	General purpose I/O pin.
CS/	71	In 5VT	3	Host parallel interface chip select, active low.
SSYNC	71	In 5VT	3	Serial Slave Synchronous Interface input sync signal.
P0.11	71	I/O 5VT DR8	3	General purpose I/O pin.
WR/	73	In 5VT	3	Host parallel interface write, active low. D7-D0 or D15-D0 data is sampled by chip on WR/ rising edge if CS/ is low.
SSDIN	73	In 5VT	3	Serial Slave Synchronous Interface input data.
P0.12	73	I/O 5VT DR8	3	General purpose I/O pin.
RD/	72	In 5VT	3	Host parallel interface read, active low. D7-D0 or D15-D0 data is output when RD/ goes low and CS/ is low. **External 100k max pull-up resistor is needed for safe ROM boot.**
MIDI_OUT2	72	Out 5VT DR8	3	Additional Serial MIDI Out. **External 100k max pull-up resistor is needed for safe ROM boot.**
P0.13	72	I/O 5VT DR8	3	General purpose I/O pin. **External 100k max pull-up resistor is needed for safe ROM boot.** **If used as input, should not be driven low by external device while ROM boot.**

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4.3.6. Versatile IOs as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MK0-MK10	76 78-84, 71-73	I/O 5VT DR8	6	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: Second Kbd contact / switch status. When SEL0=1 then MK[0-10] holds the keyboard key-on or second contact status. When SEL0=0 then MK[0-10] gives the switch status from ROW[0-3].
D8-D15	76 78-84	I/O 5VT DR8	6	Host parallel interface upper data bits when pin A1 = 1 (mode 1)
A1	71	In 5VT	6	Host parallel interface address 1: A1=0 selects mode 0 for communication/control A1=1 selects mode 1 for fast 8/16bit data transfer
XFR_RDY	72	Out DR8	6	Host parallel interface “Transfer Ready” output. When A1 = 1, this pin is reflecting status of current data read/write. Before beginning next read/write, host has to check XFR_RDY is 1
DAAD0	73	In 5VT	6	Stereo audio data input 0, I2S or MSB format.
BR0-BR3	106-109	I/O 5VT DR12	6	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: First Kbd contact / Led data. When SEL0=1 then BR[0-10] holds the keyboard key-off or first contact status. When SEL0=0 then BR[0-10] holds the led data from ROW[0-3].
BR4-BR10	111-117	I/O 5VT DR8		
DAAD7	106	In 5VT	6	Stereo audio digital input 7, I2S or MSB format.
DABD7	107	Out DR12	6	Stereo audio digital output 7, I2S or MSB format.
DAAD6	108	In 5VT	6	Stereo audio digital input 6, I2S or MSB format.
DABD6	109	Out DR12	6	Stereo audio digital output 6, I2S or MSB format.
DABD3	111	Out DR8	6	Stereo audio digital output 3, I2S or MSB format.
DAAD2	112	In 5VT	6	Stereo audio digital input 2, I2S or MSB format.
DAAD1	113	In 5VT	6	Stereo audio digital input 1, I2S or MSB format.
XCLBD1	114	In 5VT	6	External clock bit 1 for digital audio inputs DAAD[7:0].
XWSBD1	115	In 5VT	6	External word sel. Clock 1 for digital audio inputs DAAD[7:0].
XCLBD0	116	In 5VT	6	External clock bit for digital audio inputs DAAD[7:0].
XWSBD0	117	In 5VT	6	- External word select clock 0 for digital audio inputs DAAD[7:0]. - Word Clock input for audio sync. on external clock device.
ROW0-ROW3	100-103	I/O 5VT DR8	6	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: ROW signals select keyboard, switches/Leds row and external slider analog multiplexer (4051) channel. Sixteen rows combined with eleven BR/MK columns allow to control 176 keys, 176 switches, 88 Leds and 16 sliders.
DAAD5	100	In 5VT	6	Stereo audio digital input 5, I2S or MSB format.
DABD4	101	Out DR8	6	Stereo audio digital output 4, I2S or MSB format.
DABD5	102	Out DR8	6	Stereo audio digital output 5, I2S or MSB format.
DAAD4	103	In 5VT	6	Stereo audio digital input 4, I2S or MSB format.
SEL0-SEL1	68,75	I/O 5VT DR8	6	Versatile I/O pins, fully under P16 or P24 firmware control. e.g. in 2-contact keybed scanning use: If SEL0=1, BR[0-10] & MK[0-10] hold keyboard contact input data. If SEL0=0 MK[0-10] holds switch status input, BR[0-10] holds led data output. Sel1 can be used in case of kbd, with other matrix than 8*11, multiple kbd or kbd with 3 switches per key.
DAAD3	68	In 5VT	6	Stereo audio digital input 3, I2S or MSB format.
DABD0	75	Out DR8	6	Stereo audio digital output 0, I2S or MSB format.

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4.3.7. Common Memory bus as primary function

Memory bus has a common part made of MD0-MD15 and MA0-MA15 that can be shared between different memory interfaces in some Memory Config.
- In Memory Config 1, MD0-MD15, MA0-MA15 is shared between SDRAM and NOR Flash.
- In Memory Config 2, MD0-MD15, MA0-MA15 is shared between SRAM and NOR Flash.
- In Memory Config 3, MD0-MD15, MA0-MA15 is only dedicated to SDRAM.
- In Memory Config 4 & 5, MD0-MD15, MA0-MA15 is only dedicated to SRAM.
- In Memory Config 6, MD0-MD15, MA0-MA15 are not implemented.

Pin name	Pin#	Type	Mem Cfg	Description
MA0-MA15	20-23, 49-54, 56-61	Out DR12	1-5	Common Address bits for external SRAM and NOR Flash memories, up to 1Mbit (64kx16). Address (MA0-MA13) and Bank address (MA14,MA15) for external SDRAM memory.
P10.0-P10.15	20-23, 49-54, 56-61	I/O 5VT DR12 SR3	1-5	General purpose I/O pin.
MD0-MD15	29-32, 35-40, 42-47	I/O 5VT DR12	1-5	Common Data bus for external SRAM, SDRAM and NOR Flash memory.
P9.0-P9.15	29-32, 35-40, 42-47	I/O 5VT DR12	1-5	General purpose I/O pin.

4.3.8. SDR as primary function

Pin name	Pin#	Type	Mem Cfg	Description
DRCAS/	13	Out DR12	1,3	Column address strobe for external SDRAM memory
DRRAS/	14	Out DR12	1,3	Row address strobe for external SDRAM memory
DRWE/	15	Out DR12	1,3	Write enable for external SDRAM memory
DRCKE	16	Out DR12	1,3	Clock Enable for external SDRAM memory
DRDM0, DRDM1	25,26	Out DR12	1,3	Input/output mask for external SDRAM
DRCK	28	Out DR12	1,3	Positive clock for external SDRAM memory
DRCS0/	17	Out DR12	1,3	Chip select 0 for external SDRAM memory
SPICS1/	17	Out DR12	1,3	Chip select 1 for Multi-purpose Quad SPI interface..
P3.4	17	I/O 5VT DR12 SR7	1,3	General purpose I/O pin.
DRCS1/	18	Out DR12	1,3	Chip select 1 for external SDRAM memory.
XIO/_DBGCS/	18	Out DR12	1	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM. **External 100k pull-up resistor is needed for safe ROM boot.**
P3.5	18	I/O 5VT DR12 SR7	1,3	General purpose I/O pin.

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4.3.9. NOR Flash and SRAM as primary function

Pin name	Pin#	Type	Mem Cfg	Description
MA16-MA18	71-73	Out DR8	1,2,4,5	Address bits for external SRAM and NOR Flash memories, extension to 8Mbits (512kx16).
P1.0-P1.2	71-73	I/O 5VT (PD) DR8	1,2,4,5	General purpose I/O pin.
MA19-MA26	76 78-84	Out DR8	1,2	Address bits for external SRAM and NOR Flash memory, up to 2Gbit (256MByte).
XFR_RDY	83	Out DR8	1,2	Host parallel interface “Transfer Ready” output. When A1 = 1, this pin is reflecting status of current data read/write. Before beginning next read/write, host has to check XFR_RDY is 1
A1	84	In 5VT	1,2	Host parallel interface address 1: A1=0 selects mode 0 for communication/control A1=1 selects mode 1 for fast 8/16bit data transfer
P1.3-P1.10	76, 78-84	I/O 5VT (PD) DR8	1,2	General purpose I/O pin.
MWE/	74	Out DR8	1,2,4,5	External SRAM and NOR Flash memories write enable, active low.
P1.11	74	I/O 5VT (PU) DR8 SR3	1,2,4,5	General purpose I/O pin.
MOE/	75	Out DR8	1,2,4,5	External SRAM and NOR Flash memory output enable, active low.
P1.12	75	I/O 5VT (PU) DR8 SR3	1,2,4,5	General purpose I/O pin.
NRCS0/	10	Out DR12	1,2	External NOR Flash memory chip select 0, active low.
P1.13	10	I/O 5VT (PU) DR12 SR3	1,2	General purpose I/O pin.
NRCS1/	11	Out DR12	1,2	External NOR Flash memory chip select 1, active low.
P1.14	11	I/O 5VT (PU) DR12	1,2	General purpose I/O pin.
SRCS/	69	Out DR8	2,4,5	External SRAM memory chip select, active low.
P1.15	69	I/O 5VT (PU) DR8	2,4,5	General purpose I/O pin.

4.3.10. NAND Flash as primary function

Pin name	Pin#	Type	Mem Cfg	Description
NDIO0-NDIO7	111-118	I/O DR8	3,4	Data bus for external 8-bit NAND Flash memory.
NDCE0/	98	Out DR12	3,4	External NAND Flash memory chip select 0, active low
NDCE1/	99	Out DR12	3,4	External NAND Flash memory chip select 1, active low
P3.12	99	I/O 5VT (PU) DR12	3,4	General purpose I/O pin.
NDR|B/	100	In 5VT	3,4	External NAND Flash Ready Busy/ status. Indicates target array activity. External pull-up resistor is needed if NAND Flash R|B/ is open-drain output.
NDALE	101	Out DR8	3,4	External NAND Flash Address Latch Enable. Load an address from I/O[7:0] into the address register.
NDCLE	102	Out DR8	3,4	External NAND Flash Command Latch Enable. Load a command from I/O[7:0] into the command register
NDWE/	103	Out DR8	3,4	External NAND Flash Write Enable. Transfer commands, address, and serial data from SAM5704B to the NAND Flash.
NDRE/	104	Out DR8	3,4	External NAND Flash Read Enable. Transfer serial data from the NAND Flash to SAM5704B.

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4.3.11. Quad SPI NOR Flash as primary function

Pin name	Pin#	Type	Mem Cfg	Description
QNRCK	104	Out DR8	6	Data clock for QSPI NOR Flash interface.
P7.9	104	I/O 5VT 2DR8 SR3	6	General purpose I/O pin.
QNRCS0/	11	Out DR12	6	Chip select 0 for QSPI NOR Flash interface.
P1.14	11	I/O 5VT (PU) DR12 SR3	6	General purpose I/O pin..
QNRCS1/	118	Out DR8	6	Chip select 1 for QSPI NOR Flash interface.
P3.13	118	I/O 5VT (PU) DR8	6	General purpose I/O pin.
QNR0	29	I/O 5VT DR12	6	QSPI NOR Flash data 0. - Serial Output to SI peripheral Input for Single bit data commands (MOSI). - Serial IO0 for Quad operations.
P7.5	29	I/O 5VT DR12 SR3	6	General purpose I/O pin.
QNR1	30	I/O 5VT DR12	6	QSPI NOR Flash data 1. - Serial Input from SO peripheral Output for Single bit data commands (MISO). - Serial IO1 for Quad operations.
P7.6	30	I/O 5VT DR12 SR3	6	General purpose I/O pin.
QNR2-QNR3	31-32	I/O 5VT DR12	6	QSPI NOR Flash data 2-3. Serial IO2-IO3 for Quad operations
P7.7-P7.8	31-32	I/O 5VT DR12 SR3	6	General purpose I/O pin.
QNR4-QNR7	35-38	I/O 5VT DR12	6	QSPI NOR Flash data 4-7. Extension for Octal operation with two QSPI NOR Flash working in parallel. Serial IO0-IO3 for second device in Octal operations
P8.11-P8.14	35-38	I/O 5VT DR12 SR3	6	General purpose I/O pin.

4.3.12. Quad SPI SRAM as primary function

Pin name	Pin#	Type	Mem Cfg	Description
QSRCK	74	Out DR8	6	Data clock for QSPI SRAM interface.
P7.4	74	I/O 5VT DR8	6	General purpose I/O pin.
QSRCS/	10	Out 5VT DR12	6	Chip select 0 for QSPI SRAM interface.
P1.13	10	I/O 5VT (PU) DR12	6	General purpose I/O pin.
QSR0	39	I/O 5VT DR12	6	QSPI SRAM data 0. - Serial Output to SI peripheral Input for Single bit data commands (MOSI). - Serial IO0 for Quad operations.
P7.0	39	I/O 5VT DR12	6	General purpose I/O pin.
QSR1	40	I/O 5VT DR12	6	QSPI SRAM data 1. - Serial Input from SO peripheral Output for Single bit data commands (MISO). - Serial IO1 for Quad operations.
P7.1	40	I/O 5VT DR12	6	General purpose I/O pin.
QSR2-QSR3	42-43	I/O 5VT DR12	6	QSPI SRAM data 2-3. Serial IO2-IO3 for Quad operations
P7.2-P7.3	42-43	I/O 5VT DR12	6	General purpose I/O pin.

Note: This Quad SPI interface can also be used to connect a Quad SPI NOR Flash.

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4.3.13. Digital Audio as primary function

Pin name	Pin#	Type	Mem Cfg	Description
CKOUT	97	Out DR4	1-6	Audio master clock for external DAC and ADC. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, 768xFs, Fs being the DAC and ADC sampling rate.
MC0	97	In	1-6	Memory Config 0. This pin is sensed at power up. MC2|MC1|MC0 setting allows boot ROM code to start the right Memory Config.
CLBD	63	Out DR4	1-6	Audio bit clock for DABD0-DABD7 and for DAAD0-DAAD7.
FS1	63	In	1-6	Freq. Sense 1, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq. on oscillator OSC1 as follow: 00->12MHz 01->9.6MHz, 10->11.2896MHz, 11->12.288MHz
WSBD	64	I/O DR4	1-6	Out by default: Audio left/right channel select for DABD0-DABD7 and for DAAD0-DAAD7. In: WSBD from external master audio device for full audio sync without external VCXO. Same Master clock is needed on SAM5704B and external master device.
FS0	64	In	1-6	Freq. Sense 0, sensed at power up. FS1|FS0 allows boot ROM code to know operating freq on OSC1 (see FS1).
DAAD0	99	In 5VT (PD)	1,2,6	Stereo audio data input 0, I2S or MSB format.
SPDIF_IO	99	I/O 5VT (PD) DR12	1,2,6	SPDIF Input or Output. Input by default.
P2.0	99	I/O 5VT (PD) DR12	1,2,6	General purpose I/O pin.
DAAD0	10	In 5VT (PD)	3-5	Stereo audio digital input 0, I2S or MSB format.
SPDIF_IO	10	I/O 5VT (PD) DR12	3-5	SPDIF Input or Output. Input by default.
P2.0	10	I/O (PD) DR12	3-5	General purpose I/O pin.
DAAD1	68	In 5VT (PD)	1,3,5	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	68	Out DR8	1,3,5	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	68	I/O 5VT (PD) DR8	1,3,5	General purpose I/O pin.
DAAD1	18	In 5VT (PD)	2,4	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	18	Out 5VT DR12	2,4	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	18	I/O 5VT (PD) DR12	2,4	General purpose I/O pin.
DAAD1	26	In 5VT (PD)	6	Stereo audio digital input 1, I2S or MSB format.
PWM_OUT	26	Out DR12	6	Pulse Width Modulation Output for main clock enslavement on clock from SPDIF In or USB Audio
P2.1	26	I/O 5VT (PD) DR12	6	General purpose I/O pin.
DAAD2	70	In 5VT (PD)	1-4	Stereo audio digital input 2, I2S or MSB format.
MIDI_OUT2	70	Out DR8	1-4	Additional Serial MIDI Out.
P2.2	70	I/O 5VT (PD) DR8	1-4	General purpose I/O pin.
DAAD2	99	In 5VT (PD)	5	Stereo audio digital input 2, I2S or MSB format.
MIDI_OUT2	99	Out DR12	5	Additional Serial MIDI Out.
P2.2	99	I/O 5VT (PD) DR12	5	General purpose I/O pin.
DAAD3	68	In 5VT (PD)	2,4	Stereo audio digital input 3, I2S or MSB format.
P2.3	68	I/O 5VT (PD) DR8	2,4	General purpose I/O pin.
DAAD3	104	In 5VT (PD)	5	Stereo audio digital input 3, I2S or MSB format.
P2.3	104	I/O 5VT (PD) DR8	5	General purpose I/O pin.
DAAD4	103	In 5VT (PD)	2,5	Stereo audio digital input 4, I2S or MSB format.
P2.4	103	I/O 5VT (PD) DR8	2,5	General purpose I/O pin.

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Pin name	Pin#	Type	Mem Cfg	Description
DAAD5	100	In 5VT (PD)	2,5	Stereo audio digital input 5, I2S or MSB format.
P2.5	100	I/O 5VT (PD) DR8	2,5	General purpose I/O pin.
DABD0	98	Out DR12	1,2,6	Stereo audio digital output 0, I2S format.
SPDIF_OI	98	Out DR12	1,2,6	SPDIF Output or Input. Output by default.
P2.15	98	I/O 5VT DR12	1,2,6	General purpose I/O pin.
DABD0	11	Out DR12	3-5	Stereo audio digital output 0, I2S format.
SPDIF_OI	11	Out DR12	3-5	SPDIF Output or Input. Output by default.
P2.15	11	I/O 5VT DR12	3-5	General purpose I/O pin.
DABD1	69	Out DR8	1,3,6	Stereo audio digital output 1, I2S format.
XIO/_DBGCS/	69	Out DR8	1	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM.
P2.8	69	I/O 5VT (PU) DR8	1,3	General purpose I/O pin.
DABD1	26	Out DR12	2,4,5	Stereo audio digital output 1, I2S format.
XIO/_DBGCS/	26	Out DR12	2,4,5	If normal mode: Extended chip select If debug mode: Chip select for debug in external SRAM. External 100k pull-up resistor is needed for safe ROM boot.
P2.8	26	I/O 5VT DR12	2,4,5	General purpose I/O pin.
DABD2	28	Out DR12	2,4-6	Stereo audio digital output 2, I2S or MSB format.
P2.9	28	I/O 5VT DR12	2,4-6	General purpose I/O pin.
DABD3	17	Out DR12	2,4	Stereo audio digital output 3, I2S or MSB format.
P2.10	17	I/O 5VT DR12	2,4	General purpose I/O pin.
DABD3	98	Out DR12	5	Stereo audio digital output 3, I2S or MSB format.
P2.10	98	I/O 5VT DR12	5	General purpose I/O pin.
DABD4	101	Out DR8	2,5	Stereo audio digital output 4, I2S or MSB format.
P2.11	101	I/O 5VT DR8	2,5	General purpose I/O pin.
DABD5	102	Out DR8	2,5	Stereo audio digital output 5, I2S or MSB format.
P2.12	102	I/O 5VT DR8	2,5	General purpose I/O pin.
DABD6	104	Out DR8	2	Stereo audio digital output 6, I2S or MSB format.
P2.13	104	I/O 5VT DR8	2	General purpose I/O pin.

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4.4. Primary & Secondary functions quick view

4.4.1. Key table

Function Code	Function description	Available in…
1	Multi-purpose Quad SPI interface	Mem. Config. 1-6
2	Ethernet MAC	Mem. Config. 5, 6
3	Host Parallel Interface (8-bit)	Mem. Config. 1-6
4	Host Parallel Interface extension	Mem. Config. 1, 2, 6
5	UART / MIDI interface	Mem. Config. 1-6
6	Debug interface	Mem. Config. 1-6
7	Serial Slave Synchronous interface	Mem. Config. 1-6
8	I2S Digital Audio Interface	Mem. Config. 1-6 (see Note1)
9	SPDIF Digital Audio Interface	Mem. Config. 1-6
10	Versatile IOs (VIO)	Mem. Config. 6
11	Common Memory Bus	Mem. Config. 1-5
12	SDRAM controller on Memory Port 0	Mem. Config. 1, 3
13	NOR Flash and SRAM Controller on Mem. Port 0	Mem. Config. 1, 2, 4, 5 (see Note2)
14	NAND Flash Controller on Memory Port 1	Mem. Config. 3,4
15	Quad SPI NOR Flash Controller on Memory Port 1	Mem. Config. 6
16	Quad SPI SRAM Controller on Memory Port 0	Mem. Config. 6
17	USB High Speed Host, Device or Dual Role	Mem. Config. 1-6

Note1: All Digital Audio Signals are not available for each Memory Configuration.
Note2: All Signals are not available for each Memory Configuration.

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4.4.2. Functions per pin

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	TST				Config 1-6
	RST/				Config 1-6
	OSC2_X1-OSC2_X2				Config 1-6
	VIN				Config 1-6
4	MIDI_OUT1 (UART Tx)			P0,9	Config 1-6
4	MIDI_IN1 (UART Rx)	5	MIDI_IN2	P0.14	Config 1-6
5	STIN				Config 1-6
5	STOUT	5	MIDI_IN2	P0.15	Config 1-6
	Multi-purpose Quad SPI				
1	SPICK		PWM_OUT	P7.14	Config 1-6
1	SPICS0/			P7.15	Config 1-6
1	SPI0 (MOSI)	9	SPDIF_OI	P7.10	Config 1-6
1	SPI1 (MISO)	9	SPDIF_IO	P7.11	Config 1-6
1	SPI2		PWM_OUT	P7.12	Config 1-6
1	SPI3	9	SPDIF_IO	P7.13	Config 1-6
	Ethernet				
2	REF_CLK	1	SPICS1/	P8.0	Config 5,6
2	ETH_RES/	8	XWSBD1	P8.1	Config 5,6
2	RX_ER	8	XCLBD1	P8.2/INTB	Config 5,6
2	RXD0	8	DAAD6	P8.3	Config 5,6
2	RXD1	8	DAAD7	P8.4	Config 5,6
2	CRS_DV	8	DABD6	P8.5	Config 5,6
2	TXD0	8	DABD7	P8.6	Config 5,6
2	TXD1	1	SPICS2/	P8.7	Config 5,6
2	TX_EN	1	SPICS3/	P8.8	Config 5,6
2	MDC	8	XWSBD0	P8.9	Config 5,6
2	MDIO	8	XCLBD0	P8.10	Config 5,6
	Host Parallel Interface				
3	D0	8	DAAD2	P0.0	Config 1-6
3	D1	8	DABD4	P0.1	Config 1-6
3	D2	8	DABD3	P0.2	Config 1-6
3	D3	8	DABD2	P0.3	Config 1-6
3	D4	8	XWSBD1	P0.4	Config 1-6
3	D5	8	XCLBD1	P0.5	Config 1-6
3	D6	8	XWSBD0	P0.6	Config 1-6
3	D7	8	XCLBD0	P0.7	Config 1-6
3	IRQ	7	SSINT/	P0.8/INTA	Config 1-6
3	A0	7	SSCLK	P0.10	Config 1-6
3	CS/	7	SSYNC	P0.11	Config 1-6
3	WR/	7	SSDIN	P0.12	Config 1-6
3	RD/	5	MIDI_OUT2	P0.13	Config 1-6

(To be continued)

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(Continued)

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	Versatile IOs				
10	MK0-MK7	4	D8-D15		Config 6
10	MK8	4	A1		Config 6
10	MK9	4	XFR_RDY		Config 6
10	MK10	8	DAAD0		Config 6
10	BR0	8	DAAD7		Config 6
10	BR1	8	DABD7		Config 6
10	BR2	8	DAAD6		Config 6
10	BR3	8	DABD6		Config 6
10	BR4	8	DABD3		Config 6
10	BR5	8	DAAD2		Config 6
10	BR6	8	DAAD1		Config 6
10	BR7	8	XCLBD1		Config 6
10	BR8	8	XWSBD1		Config 6
10	BR9	8	XCLBD0		Config 6
10	BR10	8	XWSBD0		Config 6
10	ROW0	8	DAAD5		Config 6
10	ROW1	8	DABD4		Config 6
10	ROW2	8	DABD5		Config 6
10	ROW3	8	DAAD4		Config 6
10	SEL0	8	DAAD3		Config 6
10	SEL1	8	DABD0		Config 6
	Common Memory Bus				
11	MA0-MA15			P10.0-P10.15	Config 1-5
11	MD0-MD15			P9.0-P9.15	Config 1-5
	SDR				
12	DRRAS/				Config 1,3
12	DRCAS/				Config 1,3
12	DRWE/				Config 1,3
12	DRCKE				Config 1,3
12	DRDM0				Config 1,3
12	DRDM1				Config 1,3
12	DRCK				Config 1,3
12	DRCS0/	1	SPICS1/	P3.4	Config 1,3
12	DRCS1/		XIO/_DBGCS/	P3.5	Config 1,3
	NOR Flash and SRAM				
13	MA16-MA18			P1.0-P1.2	Config 1,2,4,5
13	MA19-MA24			P1.3-P1.8	Config 1,2
13	MA25	4	XFR_RDY	P1.9	Config 1,2
13	MA26	4	A1	P1.10	Config 1,2
13	MWE/			P1.11	Config 1,2,4,5
13	MOE/			P1.12	Config 1,2,4,5
13	NRCS0/			P1.13	Config 1,2
13	NRCS1/			P1.14	Config 1,2
13	SRCS/			P1,15	Config 2,4,5

(To be continued)

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(Continued)

Function Code	Pin Name Primary Function	Function Code	Secondary Function	GPIO	Available in…
	NAND Flash				
14	NDIO0-NDIO7				Config 3,4
14	NDCE0/				Config 3,4
14	NDCE1/			P3,12	Config 3,4
14	NDR|B/				Config 3,4
14	NDALE				Config 3,4
14	NDCLE				Config 3,4
14	NDWE/				Config 3,4
14	NDRE/				Config 3,4
	Digital Audio				
8	CKOUT				Config 1-6
8	WSBD				Config 1-6
8	CLBD				Config 1-6
8	DAAD0	9	SPDIF_IO	P2.0	Config 1-6
8	DAAD1		PWM_OUT	P2.1	Config 1-6
8	DAAD2	5	MIDI_OUT2	P2.2	Config 1-5
8	DAAD3			P2.3	Config 2,4,5
8	DAAD4			P2.4	Config 2,5
8	DAAD5			P2.5	Config 2,5
8	DABD0	9	SPDIF_OI	P2,15	Config 1-6
8	DABD1		XIO/_DBGCS/	P2.8	Config 1-6
8	DABD2			P2.9	Config 2,4-6
8	DABD3			P2.10	Config 2,4,5
8	DABD4			P2.11	Config 2,5
8	DABD5			P2.12	Config 2,5
8	DABD6			P2.13	Config 2
	Quad SPI NOR Flash				
15	QNRCK			P7.9	Config 6
15	QNRCS0/			P1.14	Config 6
15	QNRCS1/			P3.13	Config 6
15	QNR0-QNR3			P7.5-P7.8	Config 6
15	QNR4-QNR7			P8.11-P8.14	Config 6
	Quad SPI SRAM				
16	QSRCK			P7.4	Config 6
16	QSRCS/			P1.13	Config 6
16	QSR0-QSR3			P7.0-P7.3	Config 6
	USB Port				
17	OSC1_X1-OSC1_X2				Config 1-6
17	USBDP-USBDM				Config 1-6
17	USBREF				Config 1-6
17	USBID	5	MIDI_OUT2	P8,15	Config 1-6

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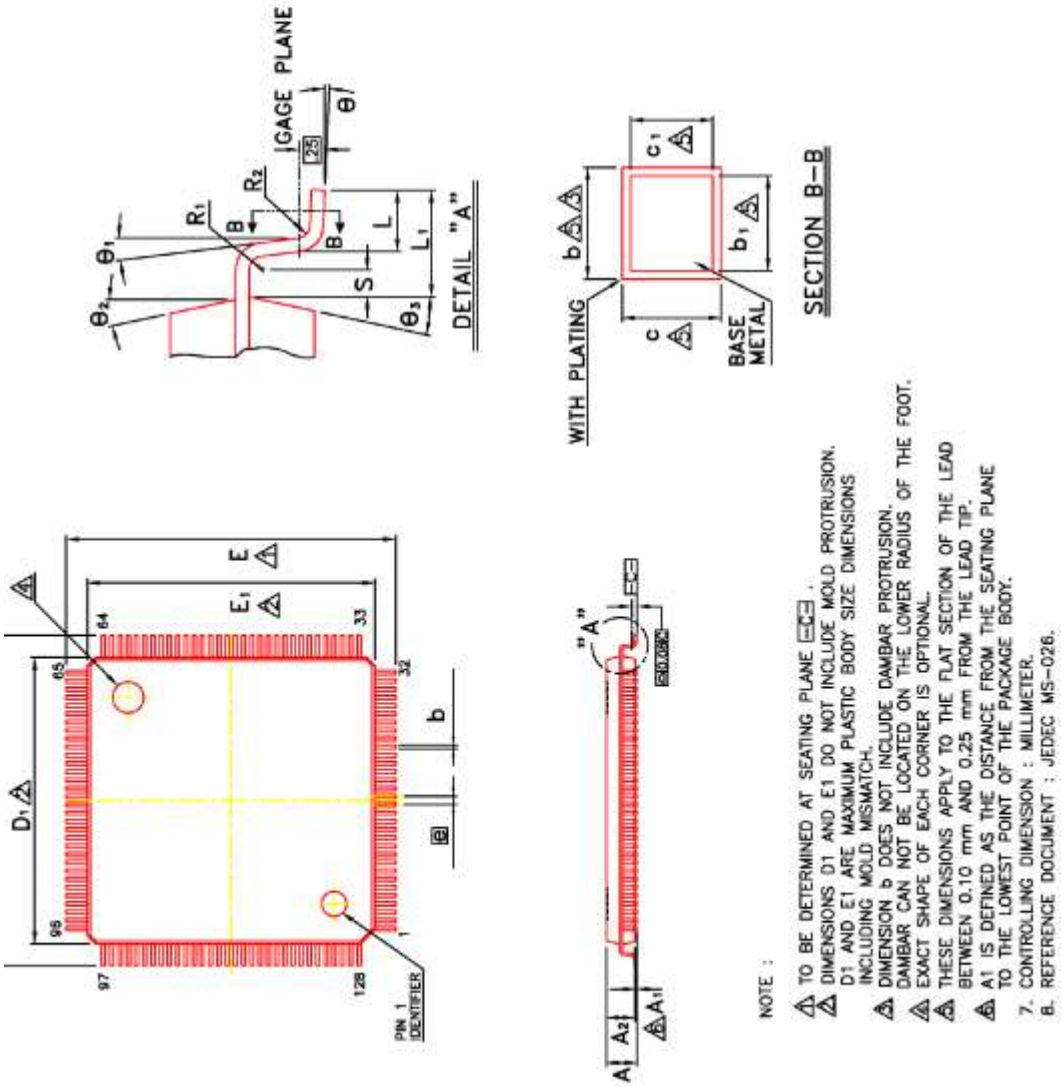
5. Mechanical dimensions

128-pin LQFP Package

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2		12°TYP			12°TYP	
θ3		12°TYP			12°TYP	



dream	ZI 21140 Semur-en-Auxois FRANCE	**TITLE:** **128LD LQFP (14 x 14 x 1.4mm)** **Package Outline -CU L/F** - L/F Material: C7025 1/2H - Foot Print : 2 mm	**Package designation** LQFP128_A	**REV.** **A**

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6. Marking

LQFP128

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7. Electrical Characteristics

7.1. Absolute Maximum Ratings(*)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature under bias	-	-55	-	+125	°C
Storage temperature	-	-65	-	+150	°C
Voltage on 5 volt tolerant pin ($_{5VT}$):	-	-0.3	-	5.5	V
Voltage on standard pin supplied by VD33:	-	-0.3	-	VD33+0.3	V
Supply voltage	VD12	-0.3	-	1.32	V
	VC12	-0.3	-	1.32	V
	VD33	-0.33	-	3.63	V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core supply voltage	VD12	1.1	1.2	1.3	V
PLL supply voltage	VC12	1.1	1.2	1.3	V
Periphery supply voltage	VD33	3	3.3	3.6	V
ADC supply voltage	VA33	3	3.3	3.6	V
Operating ambient temperature	tA	0	-	70	°C
Pull Resistor on MC[2:0] and FS[1:0] pins	RCFG	4.7k	10k	22k	Ohm

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7.3. D.C. Characteristics (TA=25°C, VD12=VC12=1.2V±10%, VD33=3.3V±10%)

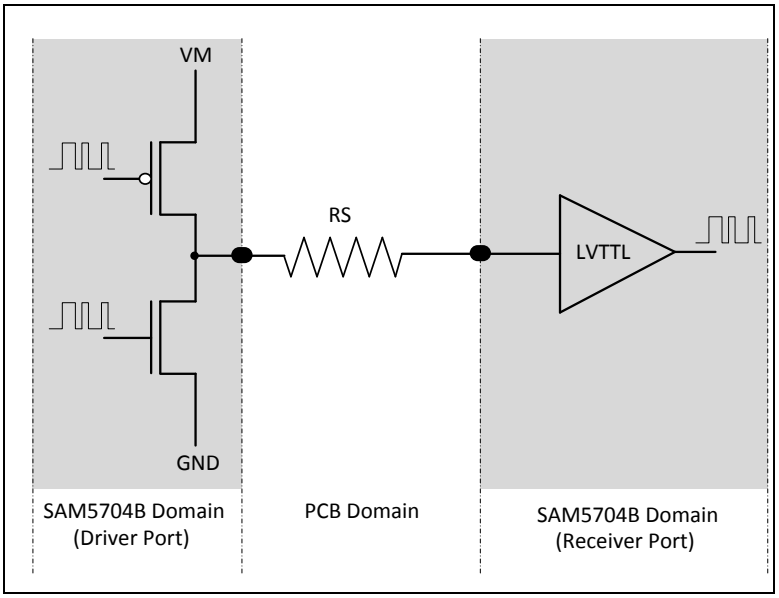
7.3.1. LVTTL pads

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-	-	0.8	V
High level input voltage on **5VT** pins	VIH	2	-	-	V
High level input voltage on non **5VT** pins	VIH	2	-	-	V
Low level output voltage (IOL =4 ~ 12mA)	VOL	-	-	0.4	V
High level output voltage (IOH =4 ~ 12mA	VOH	2.4	-	-	V
Schmitt-trigger negative-to-threshold voltage (RST/ pin)	VTN	0.8	1.1	-	V
Schmitt-trigger positive-to-threshold voltage (RST/ pin)	VTP	-	1.6	2	V
Driving capability at VOL, VOH for **DR4** pins	IOHL	-	-	4	mA
Driving capability at VOL, VOH for **DR8** pins	IOHL	-		8	mA
Driving capability at VOL, VOH for **DR12** pins	IOHL	-		12	mA
Input leakage current	IIN	-	±1	±10	µA
Built-in pull-up / pull-down resistor	RUD	40	75	190	kOhm

7.3.1.1. SDR SDRAM, FLASH or SRAM OPERATION

LVTTL pads of SAM5704B allow direct interfacing with various types of memories.

When using SDR SDRAM, FLASH or SRAM, it is recommended to use the following schematic for each connected memory pad.



VD33 = 3.3V RS = 10 Ohm
RS should be implemented in the middle of the lead-in or close to the transmitting device.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VD33	3	3.3	3.6	V
Serial resistor: High drive output	RS	8.2	10	12	Ohm

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7.3.2. Analog I/O pins (USBDP, USBDM)

Parameter	Symbol	Min	Typ	Max	Unit
High-speed differential input sensitivity VI(USBDP)-VI(USBDM)	VHSDIF	300	-	-	mV
Voltage range input of the high-speed data signaling in the common mode	VHSCM	-50	-	500	mV
High-speed idle-level output voltage (Differential)	VHSOI	-10	-	10	mV
High-speed low-level output voltage (Differential)	VHSOL	-10	-	10	mV
High-speed high-level output voltage (Differential)	VHSOH	-360	-	400	mV
Driver output impedance.	RDRV	40.5	45	49.5	Ohm

7.3.3. General Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
OUTVC12 output voltage	VD12	1.14	1.2	1.26	V
VD33 power supply current in warm power down (PLL stopped, Sys clk = 12.288MHz crystal, all P24 stopped)	ID33	-	6	-	mA
VD33 power supply current in reset mode (RST/=0)	ID33	-	0.1	-	mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped, SDR=Off)	ID33		34		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 stopped, SDR=On)	ID33		54		mA
VD33 power supply current (crystal freq.= 12.288 MHz, all P24 running, SDR=On)	ID33		96		mA
VA33 power supply current (ADC running @ 11MHz)	IA33	-	3.2	-	mA
VA33 power supply current in reset mode	IA33	-	-	<1	µA
USB Full Speed current	ID33U	-	16	-	mA
USB High Speed current	ID33U	-	29	-	mA
Ethernet MAC current	ID33E	-	15	-	mA

7.4. ADC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Analog bottom internal reference voltage	VRefN	-	100	150	mV
Analog top internal reference voltage	VRefP	VA33-175	VA33-125	-	mV
Resolution	RES	-	10	-	bit
Integral non-linearity error	INL	-2	±1	+2	LSB
Clock frequency	ADCCK	1	-	11	MHz
Sampling Rate	ADCSR	-	-	1	MSps

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8. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by a variable multiplication factor (typ. x16) to generate the internal chip system clock ("SysClk", typ. 196.6MHz @ 12.288MHz quartz).
"spck" is the period of the internal clock. Typical value with Xtal = 12.288 MHz is spck = 5.1 ns.

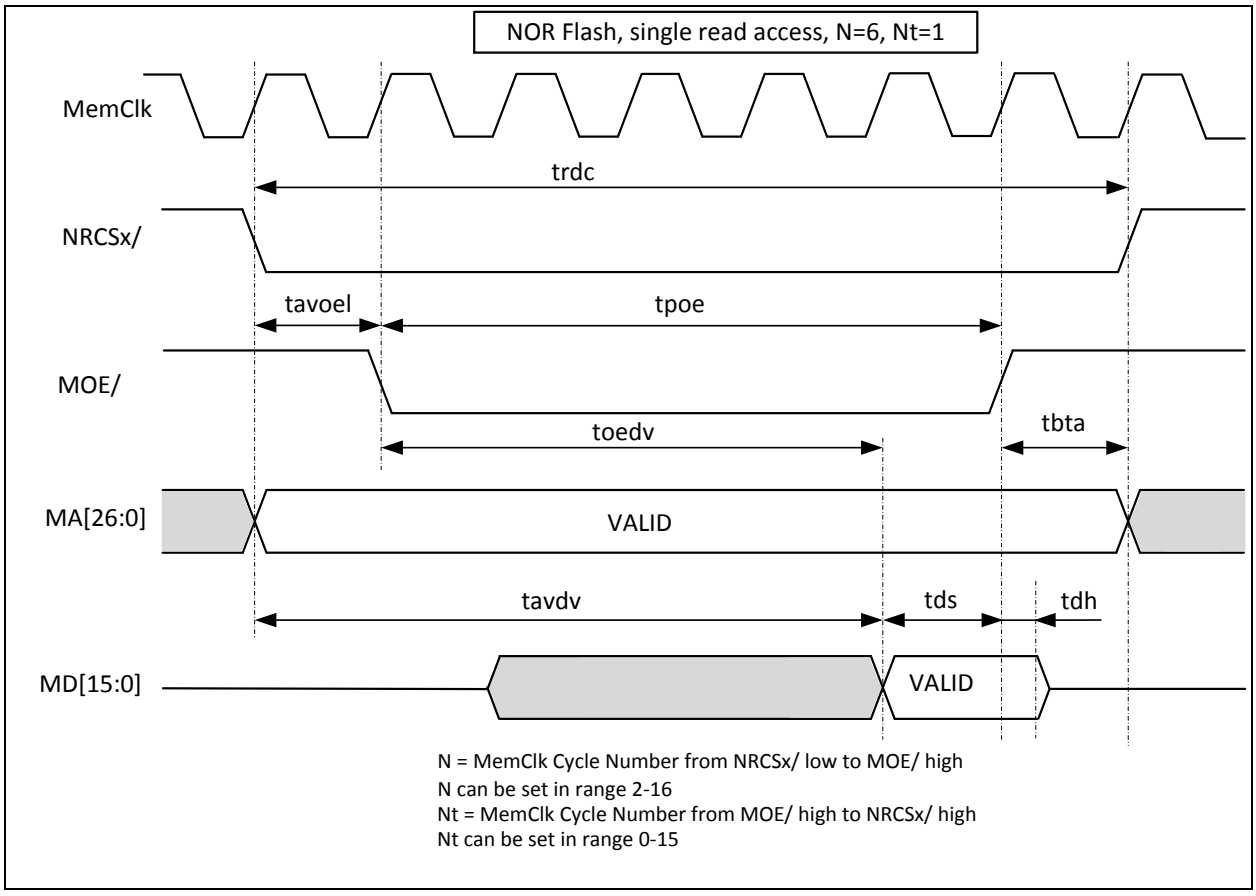
Another clock MemClk is generated from SysClk for NOR Flash, SRAM, and SDR SDRAM controllers
mpck is the period of MemClk.
mpck = spck or spck*2. Typical values with Xtal = 12.288 MHz are mpck = 10.2 ns or 5.1 ns.

8.1. NOR Flash external memory

Pins used:

MA26-MA0: Address out
MD15-MD0: Data bi-directional
NRCS0/, NRCS1/: chip select
MOE/: Output enable
MWE/: Write enable

8.1.1. NOR Flash READ CYCLE



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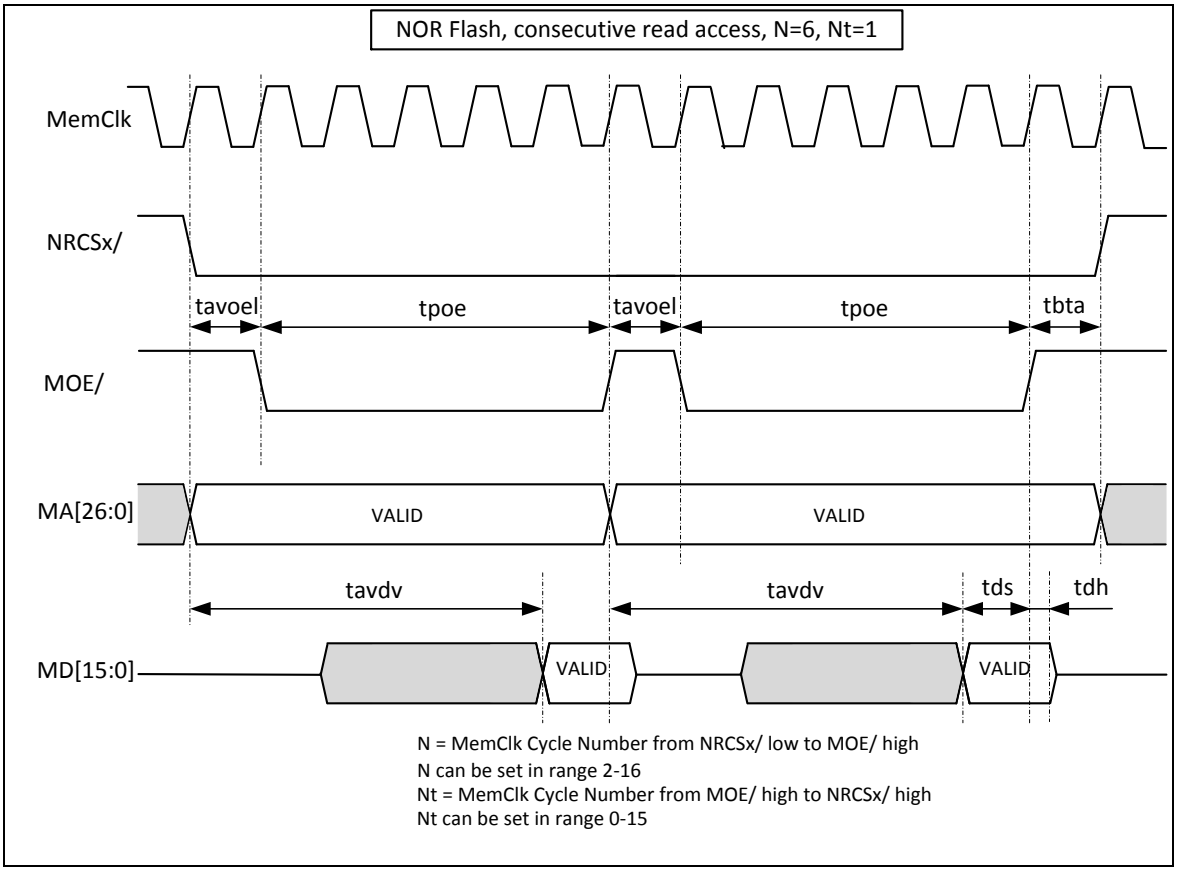

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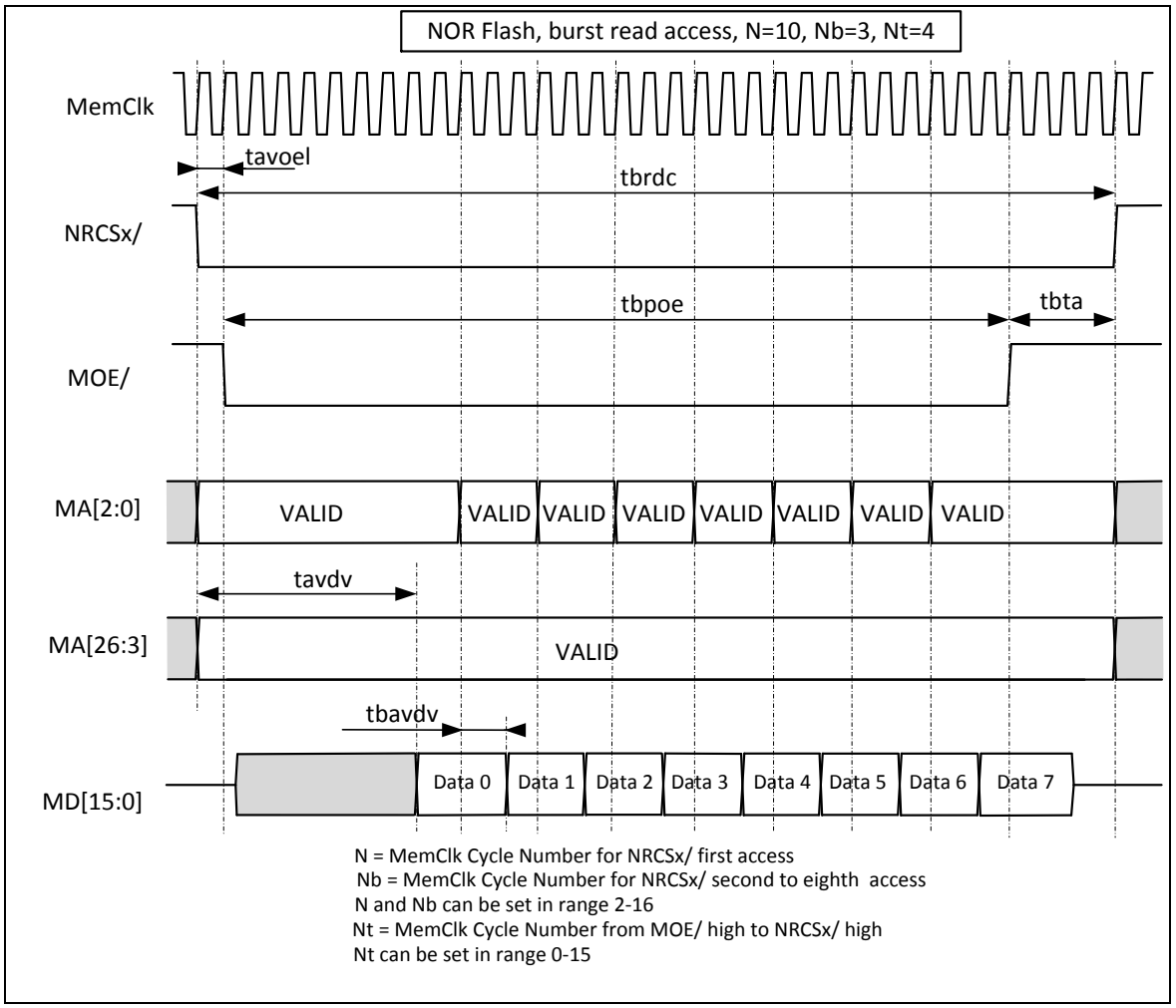

Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	trdc	-	(N+Nt)*mpck	-	ns
Read cycle time in burst mode	tbdrc	-	(N+7*Nb+Nt)*mpck	-	ns
Output enable pulse width	tpoe	(N-1)*mpck - 2.5	(N-1)*mpck	-	ns
Output enable pulse width in burst mode	tbpoe	(N-1+7*Nb)*mpck-2.5	(N-1+7*Nb)*mpck	-	ns
Chip select/address valid to data valid	tavdv	0	-	N*mpck-8.5	ns
Chip select/address valid to data valid in burst mode, access 2 to 8	tbavdv	0	-	Nb*mpck-8.5	ns
Output enable valid to data valid	toedv	0	-	(N-1)*mpck-8.5	ns
Data setup	tds	6	-	-	ns
Data hold	tdh	0	-	-	ns
Bus turnaround delay	tbta	0	Nt*mpck	-	ns
Chip select/address valid to WOE/ low	tavoel	-	mpck	-	ns

Notes:
- MemClk period = mpck
- NOR Flash random access time should be lower than tavdv Max + tds Min.
- NOR Flash page access time should be lower than tbavdv Max + tds Min.

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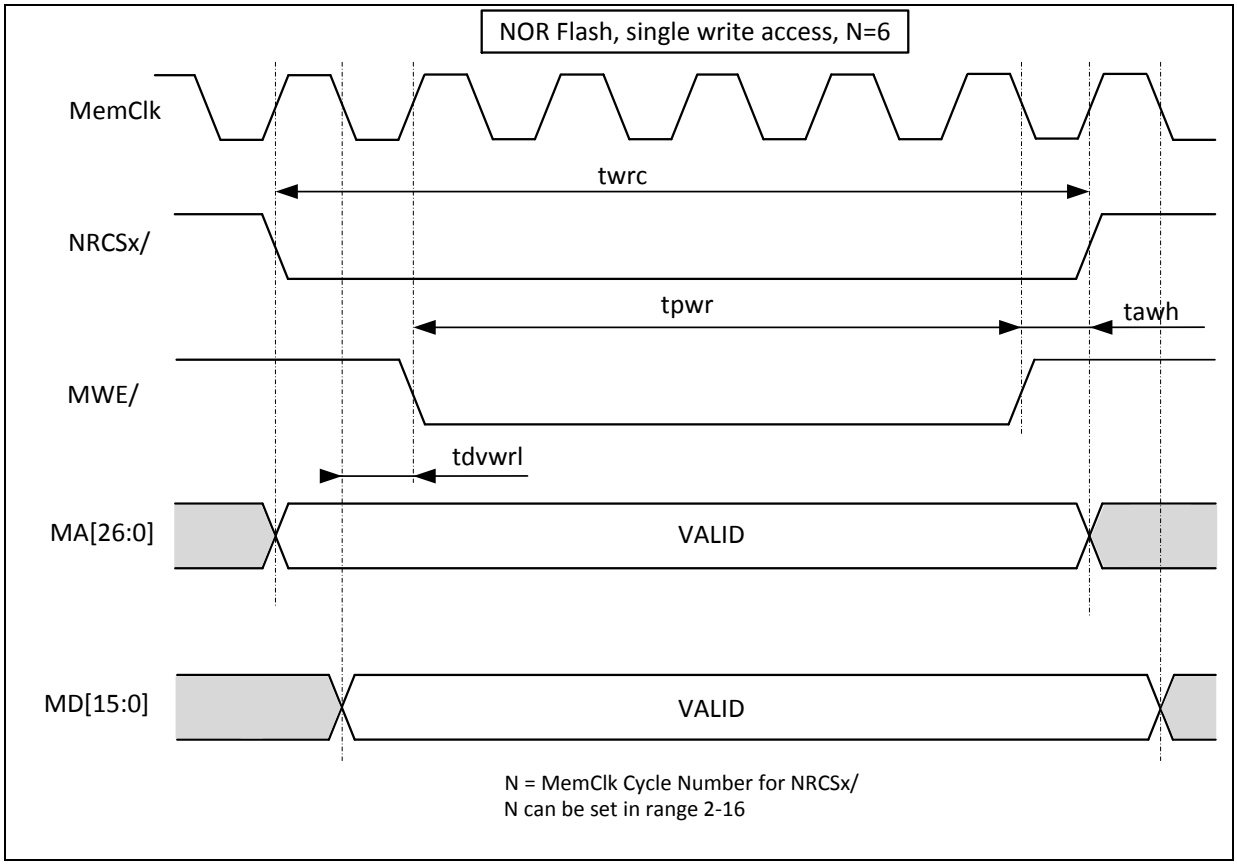
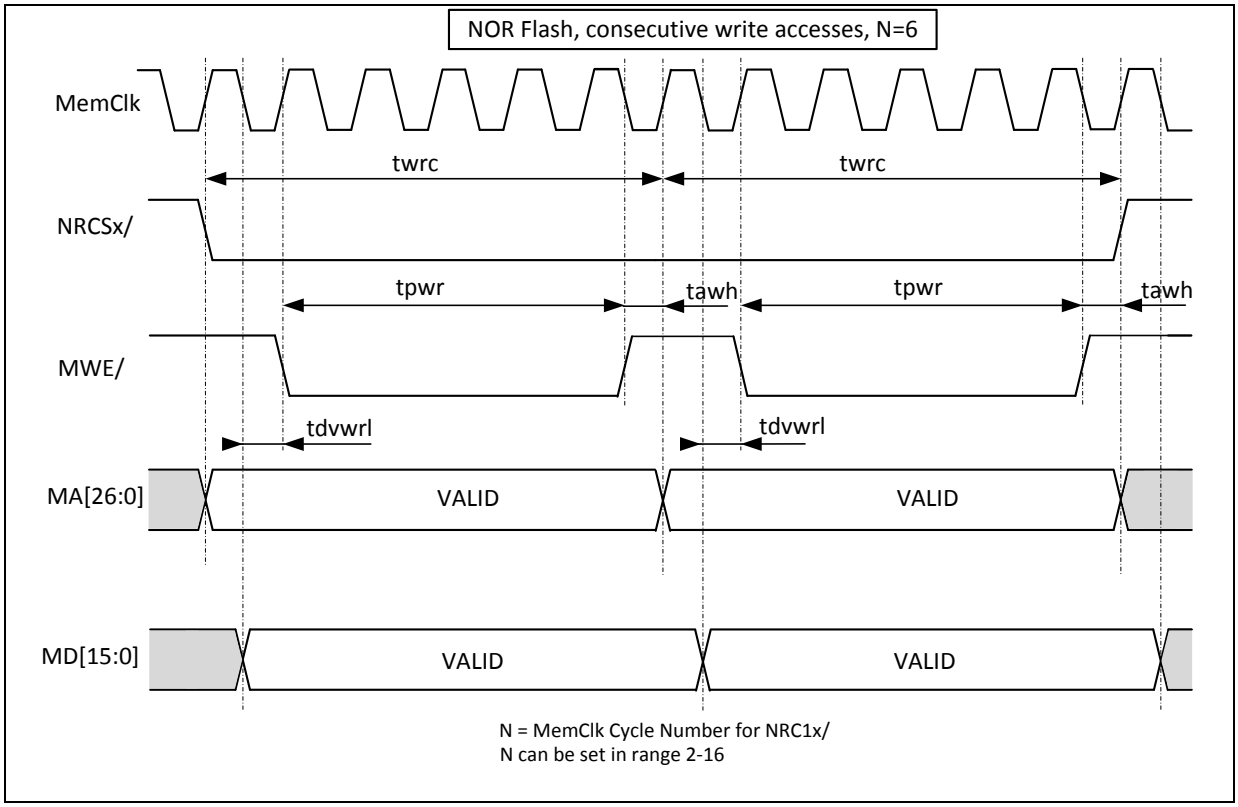
8.1.2. NOR Flash WRITE CYCLE





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Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	twrc	-	N*mpck	-	ns
Write pulse width	tpwr	(N-1.5)*mpck - 2.5	(N-1.5)*mpck		ns
Data valid to MWE/ low	tdvwrl	0.5*mpck	-	-	ns
Address out hold time	tawh	0.5*mpck- 1.5	-	-	ns

Notes:
- MemClk period = mpck

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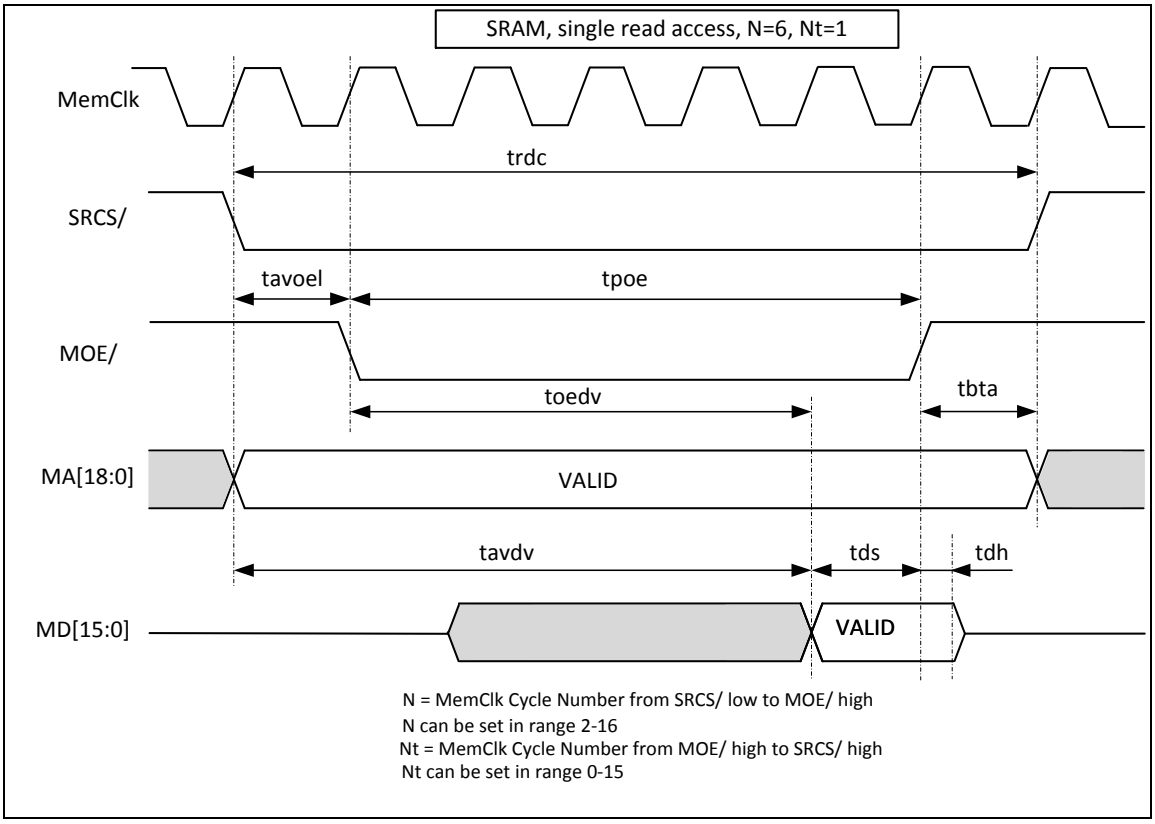
8.2. SRAM external memory

Pins used:

MA18-MA0: address out
MD15-MD0: data bi-directional
SRCS/: chip select
MOE/: output enable
MWE/: write enable

When using all address bits MA18-MA0, the maximum addressing range is 512 k x16 (8 Mbit).

8.2.1. SRAM READ CYCLE



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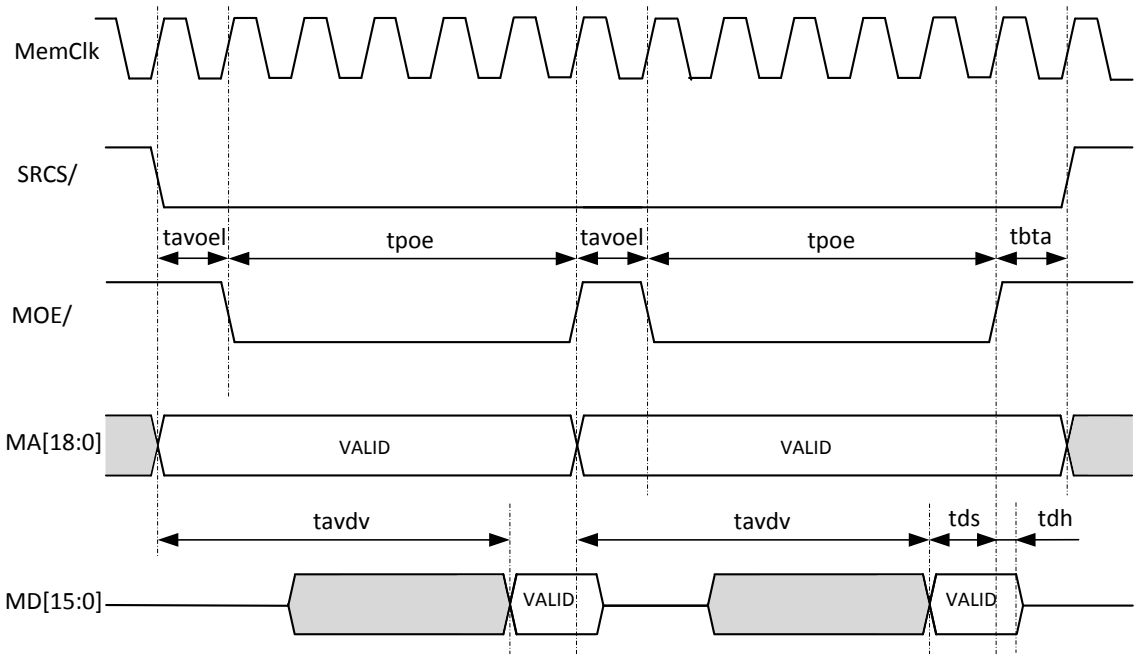
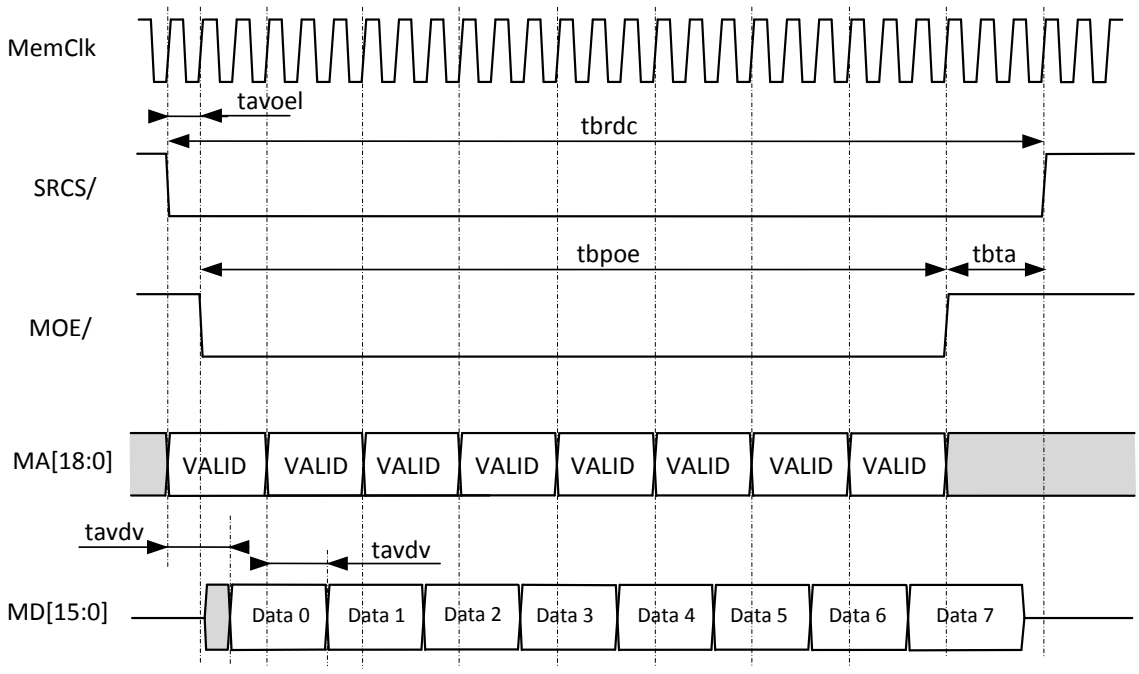
SRAM, consecutive read access, N=6, Nt=1



N = MemClk Cycle Number from SRCS/ low to MOE/ high
N can be set in range 2-16
Nt = MemClk Cycle Number from MOE/ high to SRCS/ high
Nt can be set in range 0-15

SRAM, burst read access, N=3, Nt=3



N = MemClk Cycle Number for SRCS/ first access
Nb = MemClk Cycle Number for SRCS/ second to eighth access
N and Nb can be set in range 2-16
Nt = MemClk Cycle Number from MOE/ high to SRCS/ high
Nt can be set in range 0-15

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Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	trdc	-	(N+Nt)*mpck	-	ns
Read cycle time in burst mode	tbdrc	-	(N+7*Nb+Nt)*mpck	-	ns
Output enable pulse width	tpoe	(N-1)*mpck - 2.5	(N-1)*mpck	-	ns
Output enable pulse width in burst mode	tbpoe	(N-1+7*Nb)*mpck-2.5	(N-1+7*Nb)*mpck	-	ns
Chip select/address valid to data valid	tavdv	0	-	N*mpck-8.5	ns
Output enable valid to data valid	toedv	0	-	(N-1)*mpck-8.5	ns
Data setup	tds	6	-	-	ns
Data hold	tdh	0	-	-	ns
Bus turnaround delay	tbta	0	Nt*mpck	-	ns
Chip select/address valid to WOE/ low	tavoel	-	mpck	-	ns

Notes:
- MemClk period = mpck
- SRAM access time should be lower than tavdv Max + Tds Min.

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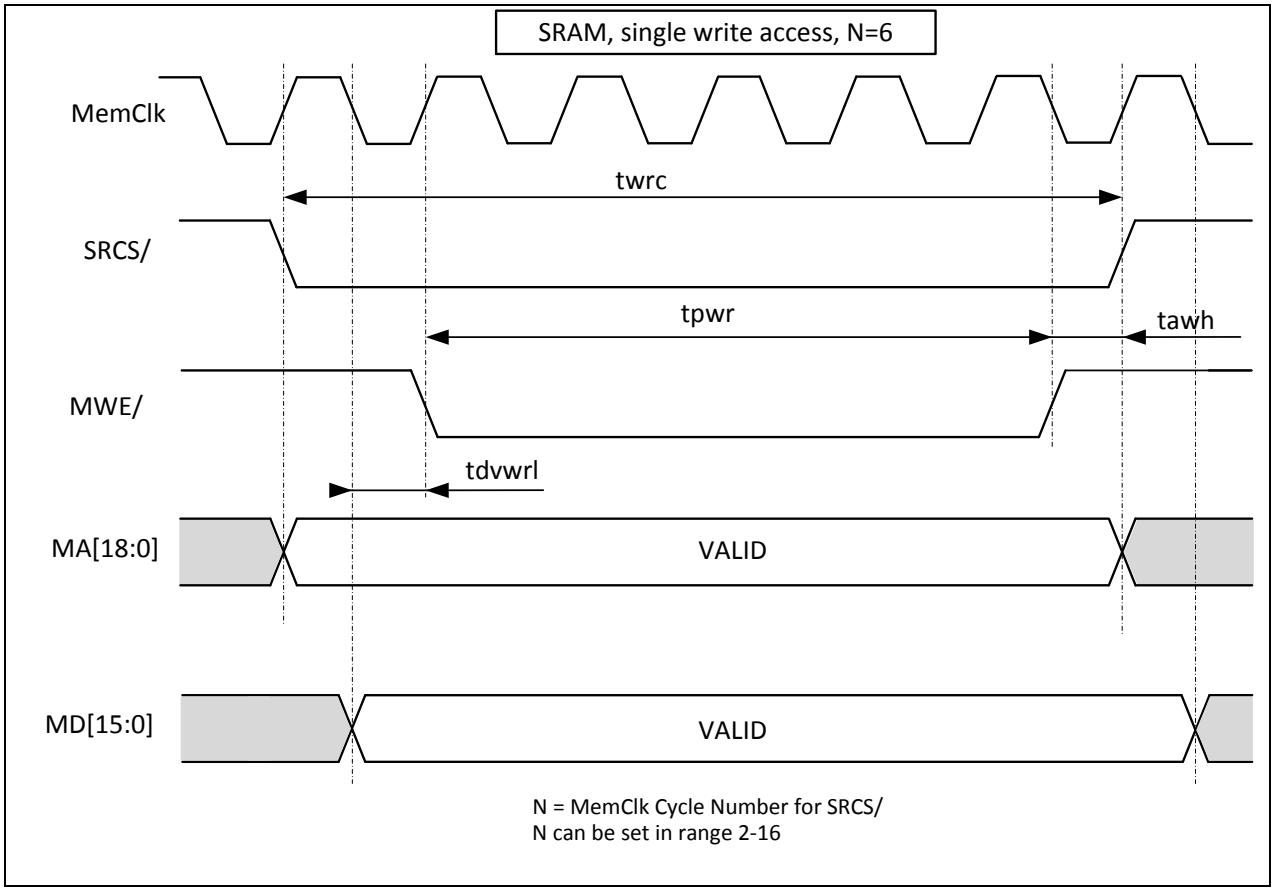
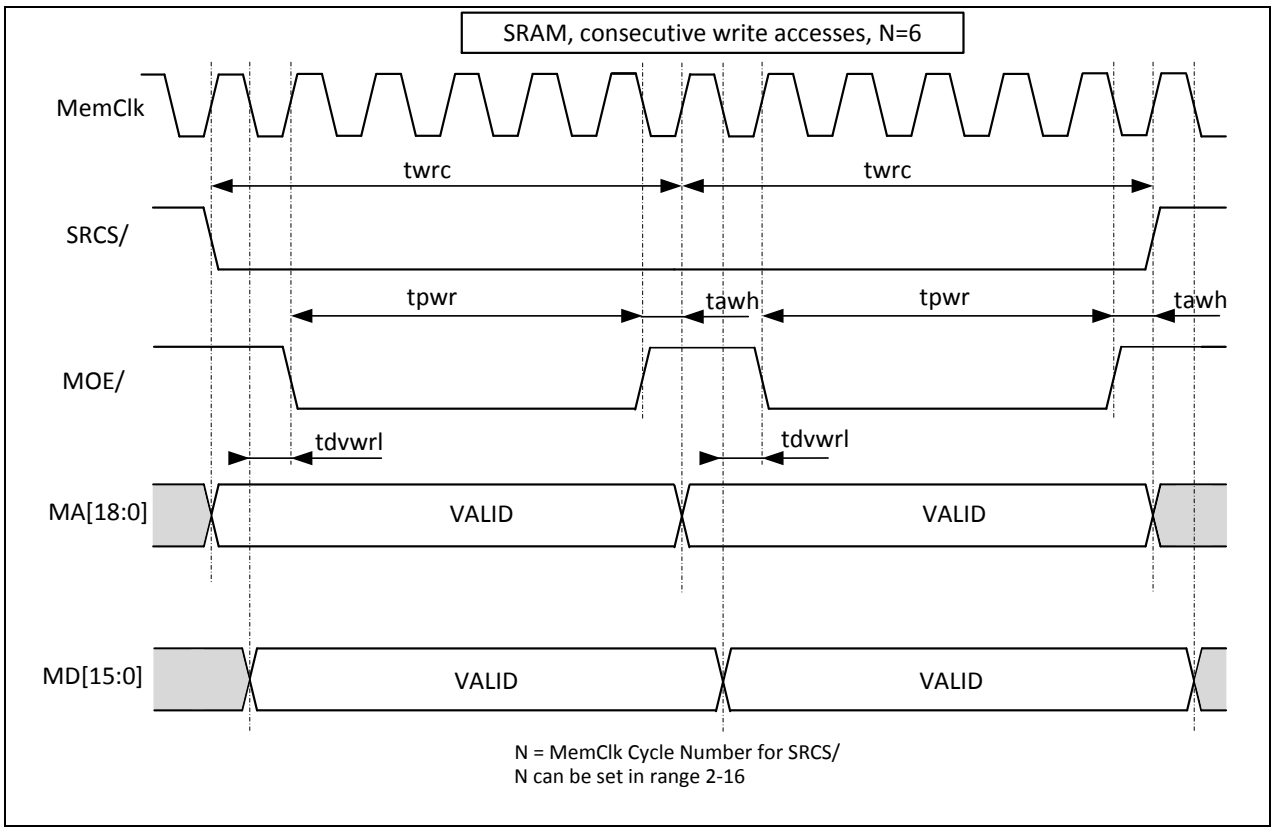
8.2.2. SRAM WRITE CYCLE





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Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	twrc	-	N*mpck	-	ns
Write pulse width	tpwr	(N-1.5)*mpck - 2.5	(N-1.5)*mpck		ns
Data valid to MWE/ low	tdvwrl	0.5*mpck	-	-	ns
Address out hold time	tawh	0.5*mpck- 1.5	-	-	ns

Notes:
- MemClk period = mpck

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8.3. External SDRAM memory

8.3.1. Overview

Following memories can be connected to the SAM5704B:

- SDR SDRAM, 16- bit wide

One or two devices can be connected on chip select DRCS0/-DRCS1/

The type of connection is LVTTL for SDRAM.

SDR SDRAM use time multiplexed addressing with a ROW/COL scheme.
MA15-MA0 are used for SDRAM.

8.3.2. Address multiplexing

Number of column address bit can be set in range 8-11.
Number of row address bit can be set in range 11-14.

8.3.3. Address connection

Below is connecting table for SDR-SDRAM device.

SDRAM address	SAM5704B address
DA0	MA0
DA1	MA1
DA2	MA2
DA3	MA3
DA4	MA4
DA5	MA5
DA6	MA6
DA7	MA7
DA8	MA8
DA9	MA9
DA10	MA10
DA11	MA11
DA12 (if available)	MA12
DA13 (if available)	MA13
BA0	MA14
BA1	MA15

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8.3.4. Address mapping examples

Example below show mapping between SAM5704B SDR address pins and address bits on SAM5704B internal ASYNC bus

SDR SDRAM 16-bit wide, 64 Mbit, 12 Row addressing, 8 Column addressing

SAM5704B address pins	ASYNC bus address bits	
	Value at RAS	Value at CAS
DRA0	AAD10	AAD0
DRA1	AAD11	AAD1
DRA2	AAD12	AAD2
DRA3	AAD13	AAD5
DRA4	AAD14	AAD6
DRA5	AAD15	AAD7
DRA6	AAD16	AAD8
DRA7	AAD17	AAD9
DRA8	AAD18	Don't care
DRA9	AAD19	Don't care
DRA10	AAD20	Auto-precharge
DRA11	AAD21	Don't care
DRBA0	AAD3	AAD3
DRBA1	AAD4	AAD4

8.3.5. Pinning

SAM5704B pin	SDR pin	Description
MA[13-0]	A[13-0]	Address
MA15, MA14	BA1, BA0	Bank address
MD[15-0]	DQ[15-0]	Data
DRDM1	DQMH	Data mask (DQ15..DQ8)
DRDM0	DQML	Data mask (DQ7..DQ0)
DRCK	CK	Clock
DRCKE	CKE	Clock enable
DRCS[1-0]	CS/	Chip select. Up to 2 devices
DRCAS/	CAS/	Command
DRRAS/	RAS/	
DRWE/	WE/	

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8.3.6. Timing

General parameters

The SDR SDRAM is used with following parameters

Parameter		Symbol	Available setting	Recommended setting
Clock cycle time		tCK	5.1ns@196.6MHz, 10.2ns@98.3MHz	10.2ns@98.3MHz
Mode Register	CAS Latency	CL	2 cycles	2 cycles
	Burst length		8 data	8 data
	Burst type		sequential	sequential
	Operating mode		normal	normal
Read delay *(programmed in SAM5704B SDRAM controller)*		RDDEL	0 to 7	≥ 3

SDR timing at 100MHz

Timing	Min	Max	To check in SDR spec
DRCK period	10 ns (100 MHz)		tCK(min)≤10 ns
Control signals output setup to rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	2.5 ns		tAS(min)≤2.5 ns tCKS(min)≤2.5 ns tCMS(min)≤2.5 ns
Control signals output hold from rising DRCK *(Control signals are DRA[13:0], DRBA[1:0], DRCS/[3:0], DRCKE, DRRAS/, DRCAS/, DRWE/)*	1.8 ns		tAH(min)≤2.5 ns tCKH(min)≤2.5 ns tCMH(min)≤2.5 ns
Data output setup to rising DRCK (write) *MD[15:0]* *DRDM[1:0]*	2.3 ns		tDS(min)≤2.3 ns
Data output and DQM hold from rising DRCK (write) *(Data Output signals are DRDQ[15:0])* *(DQM signals areDRDM[1:0]*	1.6 ns		tDH(min)≤1.6 ns
Data input delay from rising DRCK (read) *(Data Input signals are DRDQ[15:0])*	2 ns	6.4 ns	tAC(max)≤6.4 ns tOH(min)≥2 ns
Active bank A to Active bank B	8 clock cycles		tRRD(min)≤8 x tCK
Mode Register Set command cycle time	2 clock cycles		tMRD(min) ≤2 x tCK
Precharge command period during initialization	4 clock cycles		tRP(min) ≤4 x tCK
Auto-Refresh command period during initialization	24 clock cycles		tMRD(min) ≤24 x tCK

There is no hard constraint on tRFC and tREFI (outside initialization - see table above). The values specified by the component can be programmed in the controller.
There is no hard constraint on tRC, tRAS, tRCD, tWR and tRP (outside initialization - see table above). The values specified by the component must be used to compute the parameters tRBK, tWK and tRCD to be programmed in the controller.

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8.4. NAND Flash interface

8.4.1. Overview

SAM5704B can access to NAND Flash device in two ways:
- Direct communication through the NAND Flash controller. Used by P16 for NAND bad block management
- Communication through a built-in NAND Flash sequencer that will take care of transfers from the NAND Flash device to the external RAM buffer by automatically writing in NAND Flash controller registers. Used by sample cache module to feed P24 requests.

NAND Flash controller has following features:
- Handles automatic Read/write transfer through 2x2112 byte SRAM buffer
- DMA support
- Support SLC NAND Flash technology
- Programmable timing on SysClk basis
- Programmable Flash Data width 8-bit or 16-bit
- Automatic error correction while reading or writing with 4D-Hamming (up to 9 bit errors correction)
- Support Enhanced Data Output (EDO)

Pins used:
NDIO7-0: I/O for Address, Data and Command transfer on 8-bit width.
NDCE0/, NDCE1/: Chip Enable
NDALE: Address Latch Enable.
NDCLE: Command Latch Enable
NDWE/: Write Enable
NDRE/: Read Enable
NDR|B/: Ready Busy status

8.4.2. NAND Flash features

The NAND flash devices that can be used with SAM5704B need to have the following features:
- SLC technology
- ONFI compliant
- Read Cache Random (00h/31h) and Read Cache End commands support (3Fh)
- in case of multi-plane organization, it must support interleave (multi-plane) operations and must have the 'No block address restrictions' set inside its interleaved operation attributes
- 2kByte or 4kByte page size
- spare area at least 64 Bytes (for hamming ECC) by 2kBytes area
- page per block: 64,128, 256 or 512
- 5 address cycles max
- 8 GByte size max
- 8-bit bus width

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8.4.3. NAND Flash external RAM buffer

When running the NAND flash sequencer, an external RAM buffer is needed to store preloaded data. Size of this buffer depends on NAND device page size and on number of used voices.
NAND management tables (64kWord) and Sound bank parameters are also stored in this RAM.

- If NAND device page size is 2kByte
  Ext. RAM size = (Voice number x 3 x 512Word) + 64kWord + Sound Bank Parameters size

- If NAND device page size is 4kByte
  Ext. RAM size = (Voice number x 3 x 1024Word) + 64kWord + Sound Bank Parameters size

8.4.4. NAND Flash controller Timing

Timing parameters of SAM5704B NAND Flash controller are programmable. They should be set according to the parameters of the connected NAND Flash. The table below helps to make the correspondence between timing parameters used by ONFI standard and timing parameters needed by the controller. The lower case parameters refer to the controller, the upper case parameters refer to ONFI standard. This table does not take in account the propagation delays on PCB.
In the tables below, the following SAM5704B timings are used:

- tasym: Asymmetry on SAM5704B output delays (estimation: 2 ns)
- tprop: Propagation delay inside SAM5704B (max 8 ns)

SAM5704B timing parameter	Available settings	Description	NAND Flash ONFI timing
twp	(1 to 16)* spck	Write low pulse	max(tWP, tDS) + tasym
twh	(1 to 16)* spck	Write high pulse	max(tCLH, tCH, tALH, tDH, tWH, tWC-twp) + tasym
trp	(1 to 16)* spck	Read low pulse	max(tRP, tREA) + tasym
treh	(1 to 16)* spck	Read high pulse	max(tREH, tRC-trp) + tasym
bta	(1 to 64)* spck	Bus turnaround after read	tRHZ + tasym
twsetup	(1 to 16)* spck	Write setup	max(tCLS, tCS, tALS) - twp + tasym
trsetup	(1 to 16)* spck	Read setup	max(tCEA-tREA, tCLR) + tasym
tbusy	(1 to 32)* spck	Delay after busy high	tRR – trsetup
twhr	(1 to 16)* spck	Write hold	tWHR - trsetup + tasym
tceh	(1 to 8)* spck	NDCE/ high pulse	Not constrained
ce_intercept	Disable, Enable	NDCE/ intercept enable	Disable
ce_busy	Low, High	NDCE/ level during busy	High

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8.5. Multi-purpose Quad SPI interface

This is a master synchronous serial interface, operating in Single or Quad SPI mode 0.
Quad SPI modes is driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

Single SPI mode can be driven by the QSPI controller, but also by a Simple SPI interface through two IO registers.

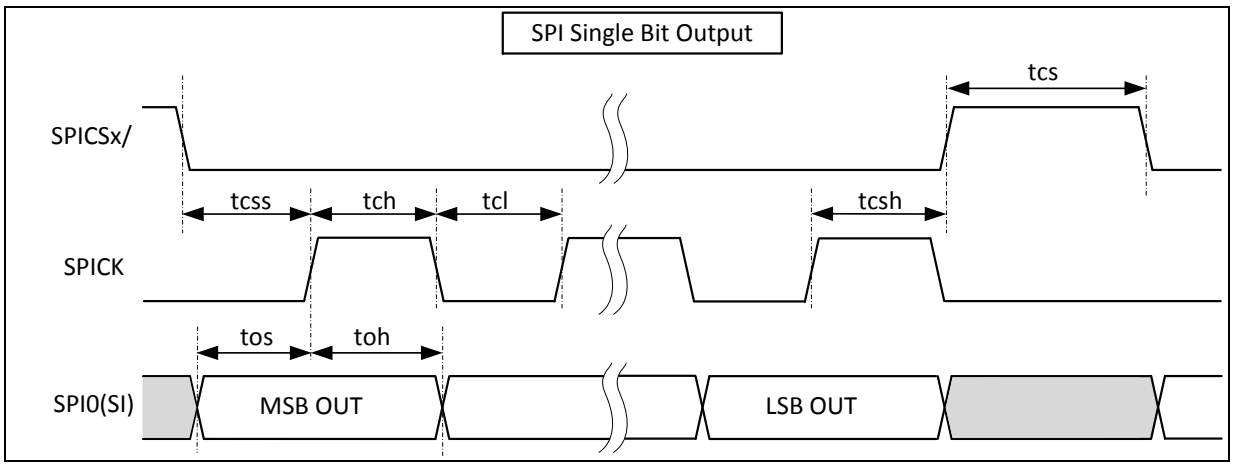
Pins used in Single SPI:

SPICK: Clock output
SPICS0/, SPICS1/, SPICS2/, SPICS3/: Chip select for up to 4 devices
SPI0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
SPI1: Serial Input to be connected to SO output of SPI peripheral (MISO)

Pins used in Quad SPI:

SPICK: Clock output
SPICS0/, SPICS1/, SPICS2/, SPICS3/: Chip select for up to 4 devices
SPI0: Serial IO0 for Quad commands and data
SPI1: Serial IO1 for Quad commands and data
SPI2: Serial IO2 for Quad commands and data
SPI3: Serial IO3 for Quad commands and data

8.5.1. Timing



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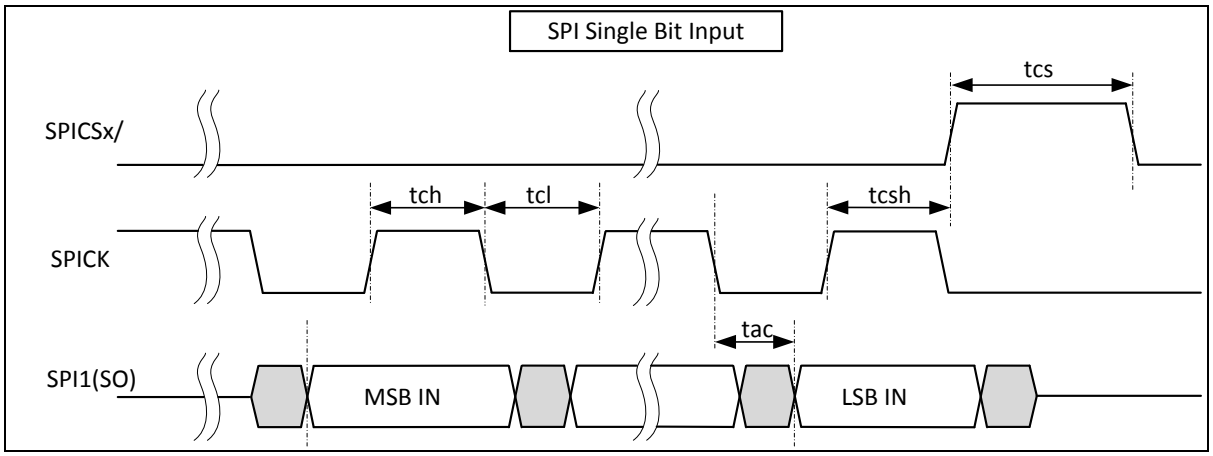

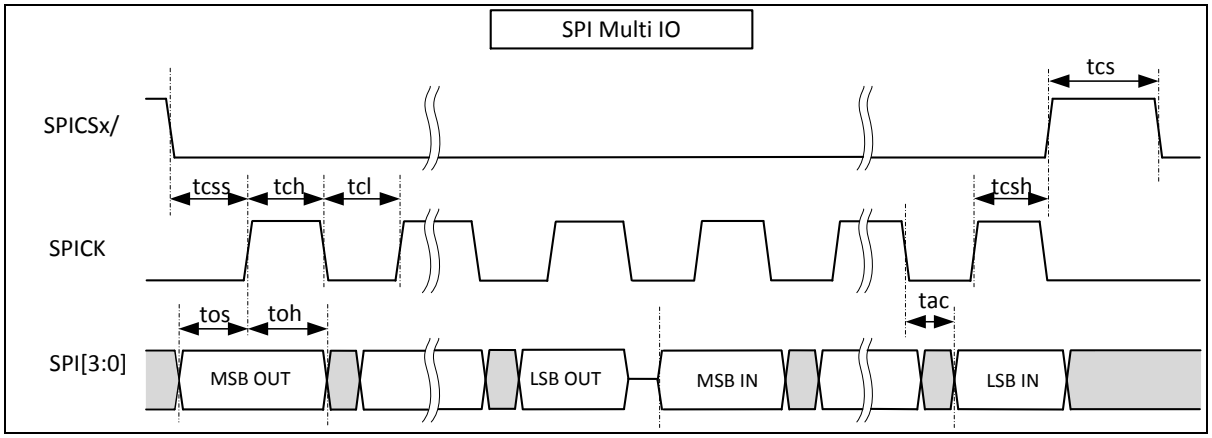

The QSPI controller works on SysClk (usually 196.608MHz with Xtal = 12.288MHz).
SPICK frequency is SysClk/Nq. Nq can be programmed between 2 and 4096.

Parameter	Symbol	Min	Typ	Max	Unit
SPICK Frequency	fspick	SysClk/4096	-	SysClk/2	Hz
Clock High Time (even Nq)	tch	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock High Time (odd Nq)	tch	0.5*spck*(Nq-1)-0.5		0.5*spck*(Nq-1)+0.5	ns
Clock Low Time (even Nq)	tcl	0.5*spck*Nq-0.5		0.5*spck*Nq+0.5	ns
Clock Low Time (odd Nq)	tcl	0.5*spck*(Nq+1)-0.5		0.5*spck*(Nq+1)+0.5	ns
CS/ High Time	tcs	spck*Nq-1.5			ns
CS/ Active Setup Time (relative to SPICK)	tcss	spck*Nq-1.5			ns
CS/ Active Hold Time (relative to SPICK)	tcsh	spck*Nq-2.5			ns
IO Out Setup Time(even Nq)	tos	0.5*spck*Nq-1.5			ns
IO Out Setup Time(odd Nq)	tos	0.5*spck*(Nq+1)-1.5			ns
IO Out Hold Time(even Nq)	toh	0.5*spck*Nq-2.5			ns
IO Out Hold Time(odd Nq)	toh	0.5*spck*(Nq-1)-2.5			ns
Access Time from falling clock edge	tac	0.5		Spck*Nq-2.5	ns

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8.6. Quad SPI NOR Flash interface

This is a master synchronous serial interface Quad SPI mode0, usually dedicated to audio samples import from Quad SPI NOR Flash.
Standard operating modes are Quad SPI and Octal SPI. However, Single SPI mode is also allowed.
Octal SPI mode is made by using two Quad SPI NOR Flash devices in parallel.

Quad and Octal SPI modes are driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

Pins used in Single SPI:

QNRCK: Clock output
QNRCS0/, QNRCS1/: Chip select for 2 devices
QNR0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
QNR1: Serial Input to be connected to SO output of SPI peripheral (MISO)

Pins used in Quad SPI:

QNRCK: Clock output
QNRCS0/, QNRCS1/: Chip select for 2 devices
QNR0: Serial IO0 for Quad commands and data
QNR1: Serial IO1 for Quad commands and data
QNR2: Serial IO2 for Quad commands and data
QNR3: Serial IO3 for Quad commands and data

Pins used in Octal SPI:

QNRCK: Clock output
QNRCS0/: First Chip select for 1 Quad Flash device low and 1 Quad Flash device high
QNRCS1/: Second Chip select for 1 Quad Flash device low and 1 Quad Flash device high
QNR3-0: Serial IO3-0 of low Quad Flash device(s) for low nibble of Octal commands and data
QNR7-4: Serial IO3-0 of high Quad Flash device(s) for high nibble of Octal commands and data

8.6.1. Timing

Timing characteristics of Quad SPI NOR Flash interface are identical to timing characteristics of Multi-purpose Quad SPI interface. See §8.5.1.

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8.7. Quad SPI SRAM interface

This is a master synchronous serial interface Quad SPI mode0, usually dedicated to effect processing in external Quad SPI SRAM. However, this interface can also be used to connect a Quad SPI NOR Flash.

Standard operating mode is Quad SPI but Single SPI mode is also allowed.

Quad SPI mode is driven by a powerful QSPI controller with following features:
- Handles automatic Read/write transfer through standard P16 instructions
- Programmable address and data formats
- Programmable data bit number
- Programmable clock up to 100MHz
- Multi-burst mode

Pins used in Single SPI:

QSRCK: Clock output
QSRCS/: Chip select
QSR0: Serial Output to be connected to SI input of SPI peripheral (MOSI)
QSR1: Serial Input to be connected to SO output of SPI peripheral (MISO)

Pins used in Quad SPI:

QSRCK: Clock output
QSRCS/: Chip select
QSR0: Serial IO0 for Quad commands and data
QSR1: Serial IO1 for Quad commands and data
QSR2: Serial IO2 for Quad commands and data
QSR3: Serial IO3 for Quad commands and data

8.7.1. Timing

Timing characteristics of Quad SRAM interface are identical to timing characteristics of Multi-purpose Quad SPI interface. See §8.5.1.

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8.8. Host Parallel Interface

This interface is used to connect the SAM5704B to an external host processor for control and fast data transfer.

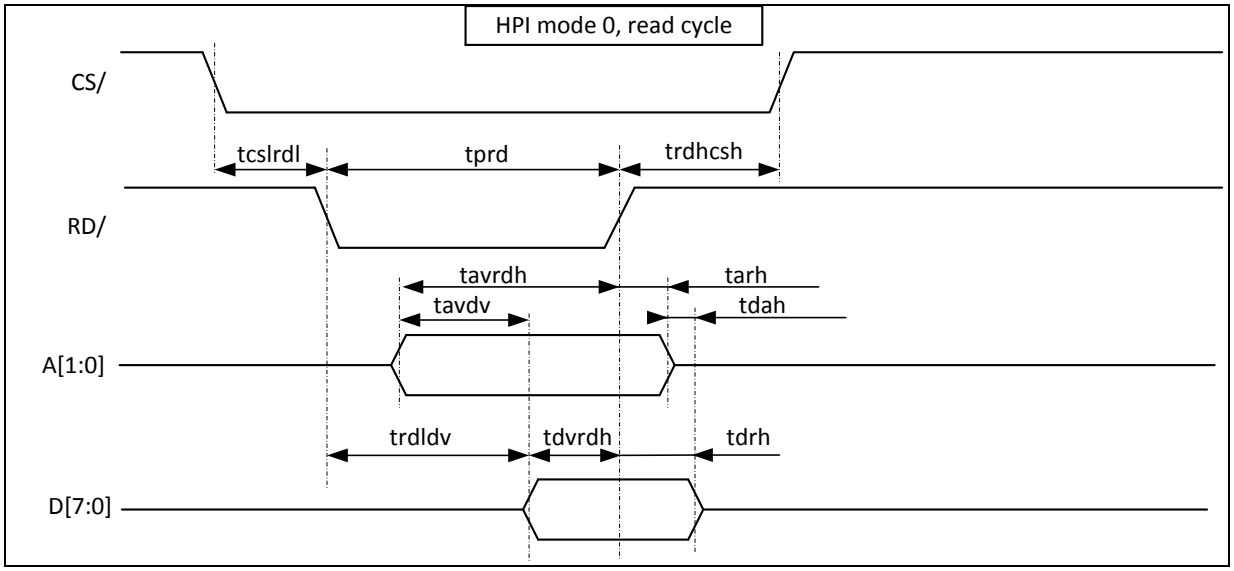
8.8.1. Host Parallel Interface (HPI) mode 0

Pins used in mode 0 (A1=0):

D7-D0: 8-bit Data I/O
CS/: Chip Select from host (input)
A1-A0: Addresses from host (input), A1=0 to select mode 0, A0 for data selection
WR/: Write from host (input)
RD/: Read from host (input)
IRQ (optional): Interrupt Request (output)

This mode is typically used to send MIDI messages or other control data from the Host CPU (master) to the SAM5704B (slave).

8.8.1.1. HPI mode 0, Timings



Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to RD/ low	tcslrdl	2	-	-	ns
RD/ pulse width	tprd	10	-	-	ns
RD/ high to CS/ high	trdhcsh	3	-	-	ns
Address valid to RD/ high	tavrdh	3	-	-	ns
Address valid to data valid	tavdv	-	-	10	ns
RD/ low to data valid	trdldv	-	-	10	ns
Data valid to RD/ high	tdvrdh	3	-	-	ns
Address out hold from RD/	tarh	3	-	-	ns
Data out hold from RD/	tdrh	0	-	10	ns
Data out hold from address out	tdah	0	-	10	ns

Notes:

1. tcslrdl Min and trdhcsh Min can be reduced to 0 ns if 3 ns are added to tprd Min, tarh Min, tdrh Min, tavrdh Min, tdvrdh Min

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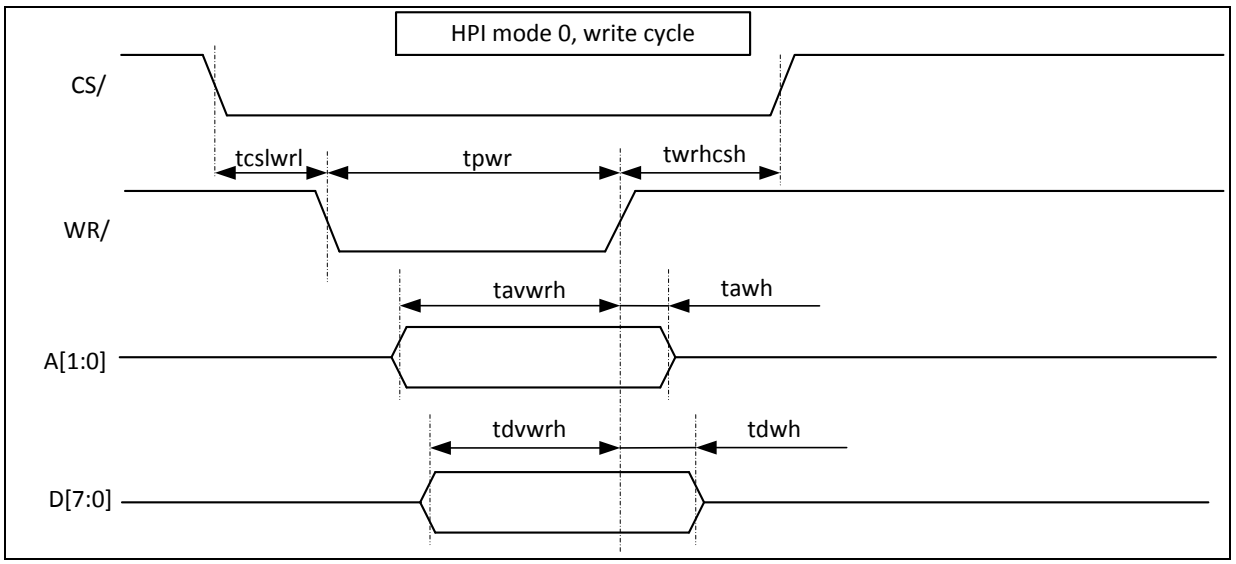

Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to WR/ low	tcslwrl	2	-	-	ns
WR/ pulse width	tpwr	5	-	-	ns
WR/ high to CS/ high	twrhcsh	3	-	-	ns
Address valid to WR/ high	tavwrh	3	-	-	ns
Data valid to WR/ high	tdvwrh	3	-	-	ns
Address out hold from WR/	tawh	3	-	-	ns
Data out hold from WR/	tdwh	3	-	-	ns

Notes:

1. tcslwrl Min and twrhcsh Min can be reduced to 0 ns if 3 ns are added to tpwr Min, tawh Min, tdwh Min, tavwrh Min, tdvwrh Min

8.8.1.2. HPI mode 0, IO Status Register

TE	RF	X	X	ID3	ID2	ID1	ID0

Status register is read when A1=0, A0=1, RD/=0, CS/=0

- TE: Transmit Empty: This bit is 1 when nothing is transmitted from SAM5704B to host. If 0, data from SAM5704B to host is pending and IRQ pin is high. Host reading the data with pin A0=0 sets TE to 1 and clear IRQ. TE bit is actually reflecting inverted value of IRQ pin (IRQ/).
- RF: Receiver Full: Host should not write any data or control to SAM5704B if this bit is 1. When 0, then SAM5704B is ready to accept data from host.
- ID[3:0]: these 4 bits are firmware dependant and may be used for defining type of data sent by SAM5704B in case of multiple flows of data.

Host read should be performed with following steps:
a) Nothing to read if IRQ pin is low. First wait for IRQ pin being high
b) Read status (A0=1) to get ID[3:0] (this step is optional if ID[3:0] bits are not used and not defined by firmware)
c) Read data (A0=0) (IRQ goes low at the end of read cycle, on rising edge of RD/ signal)
d) Wait for IRQ pin being high again…
Note: On steps a) and d), if IRQ pin is not connected and not used, host can also read status and wait for TE bit=0

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Host write should be done with following steps:
a) Read status (A0=1). If bit RF=0, go to step b). If bit RF=1, read again status till bit RF going to 0.
b) Write new data (A0=0) or new control (A0=1)

Note about step a):
There are two different cases for RF bit being 1:
- RF bit is 1 because FIFO of P16 is full. RF bit will go low again as soon as P16 is reading some bytes of the FIFO in order to have some free space again inside fifo and then is clearing bit 7 (FIFULL) of port 1 (CONTROL/STATUS). This time is firmware dependant.
- RF bit is 1 because previous host write has still not been written into the P16 FIFO. This case can happen if P16 is executing a long instruction. The writing will be indeed performed only when P16 has finished the instruction.

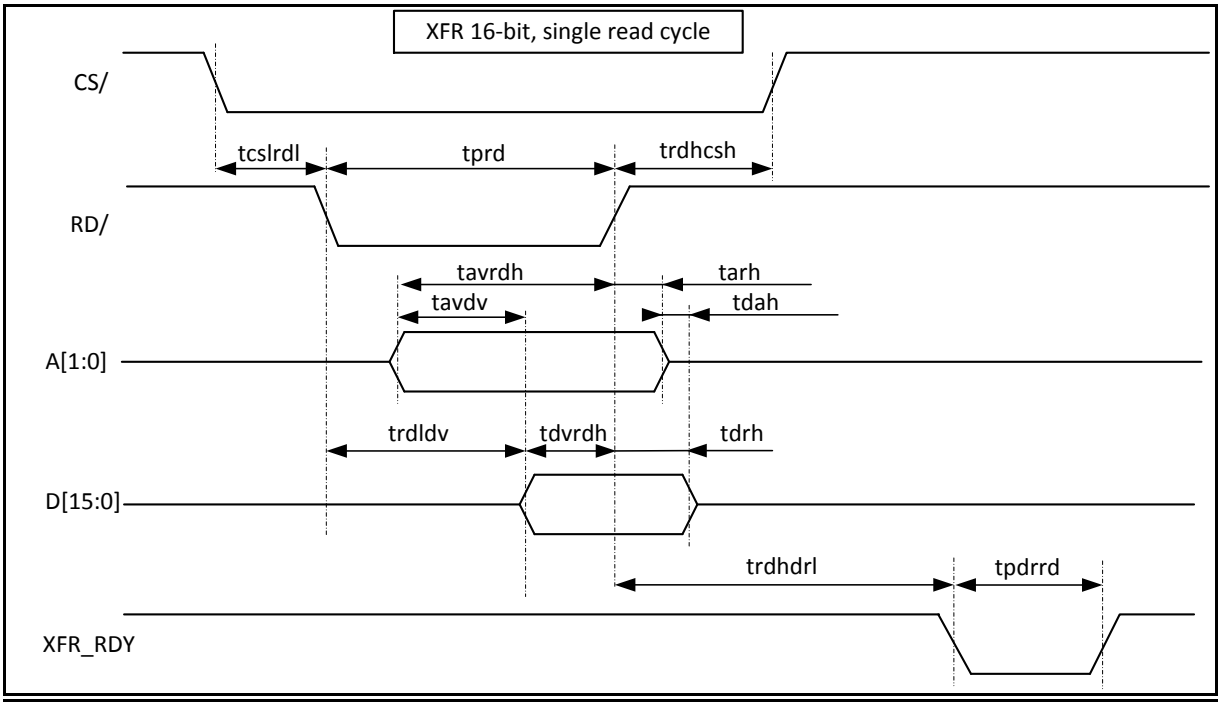
8.8.2. Host Parallel Interface mode 1 (fast data transfer)

Pins used in mode 1 (A1=1):

D7-D0 or D15-D0 (I/O)
CS/ (input)
A1-A0 (input): Addresses from host (input), A1=1 to select mode 1, A0 is “don’t care”.
WR/ (input)
RD/ (input)
XFR_RDY (output)

This interface is used for fast read/write transfer between host processor and SAM5704B. Typical applications are direct fast sound bank transfer from host to SDRAM and streaming audio.
However, any other devices connected to internal async bus of SAM5704B can be also accessed by host through this interface (other external memories, internal ram, router and P24 memories, etc…). Single or burst read/write modes are available. Read/write mode is selected by firmware

8.8.2.1. Host Parallel Interface mode 1 Read Timing



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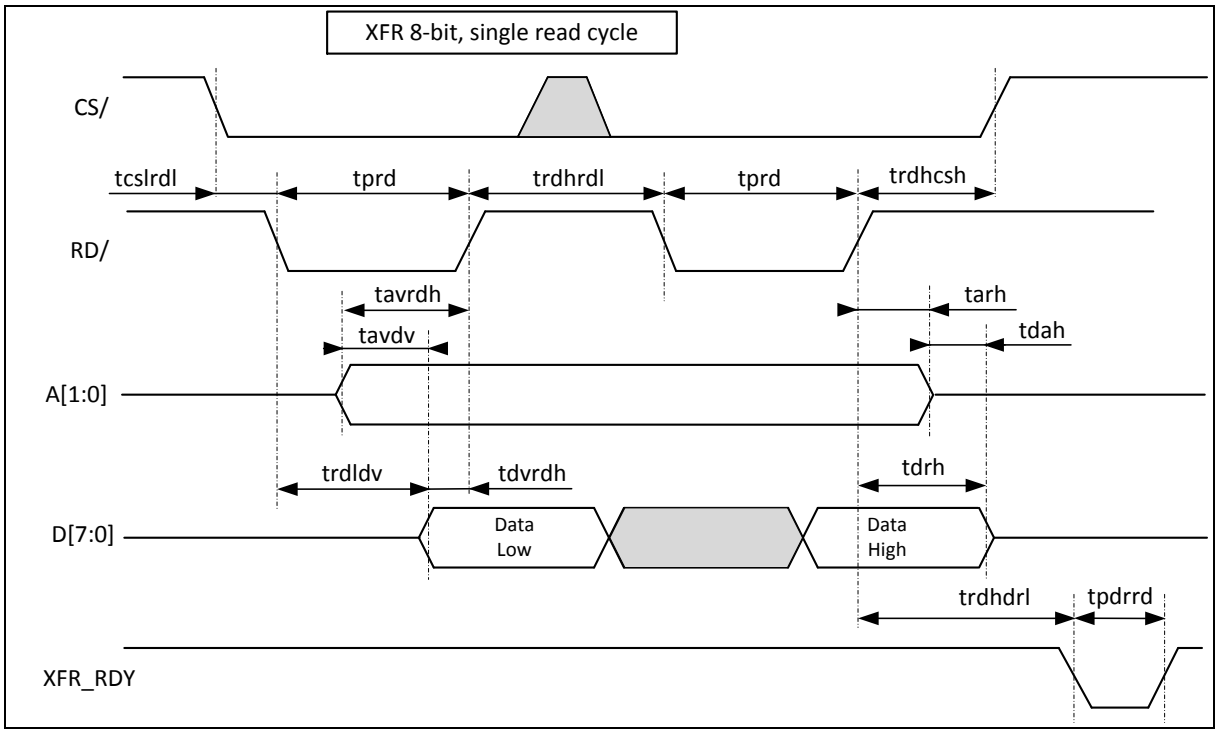

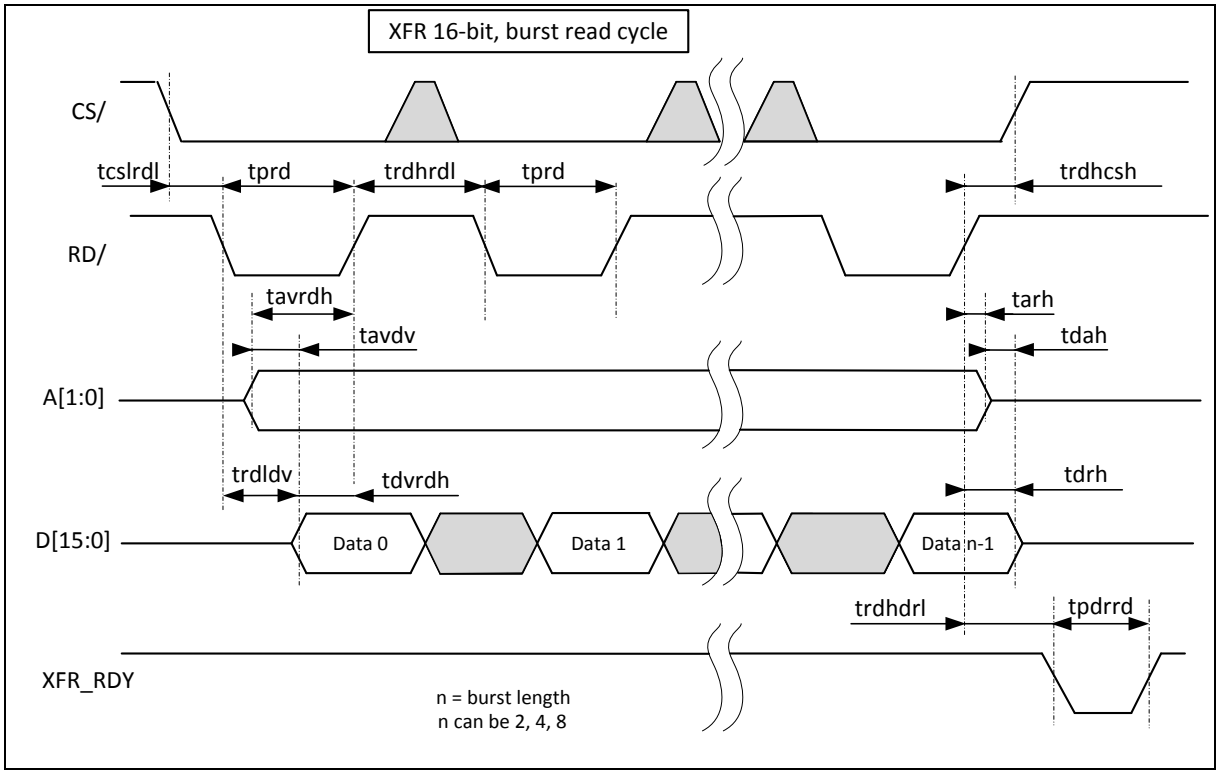

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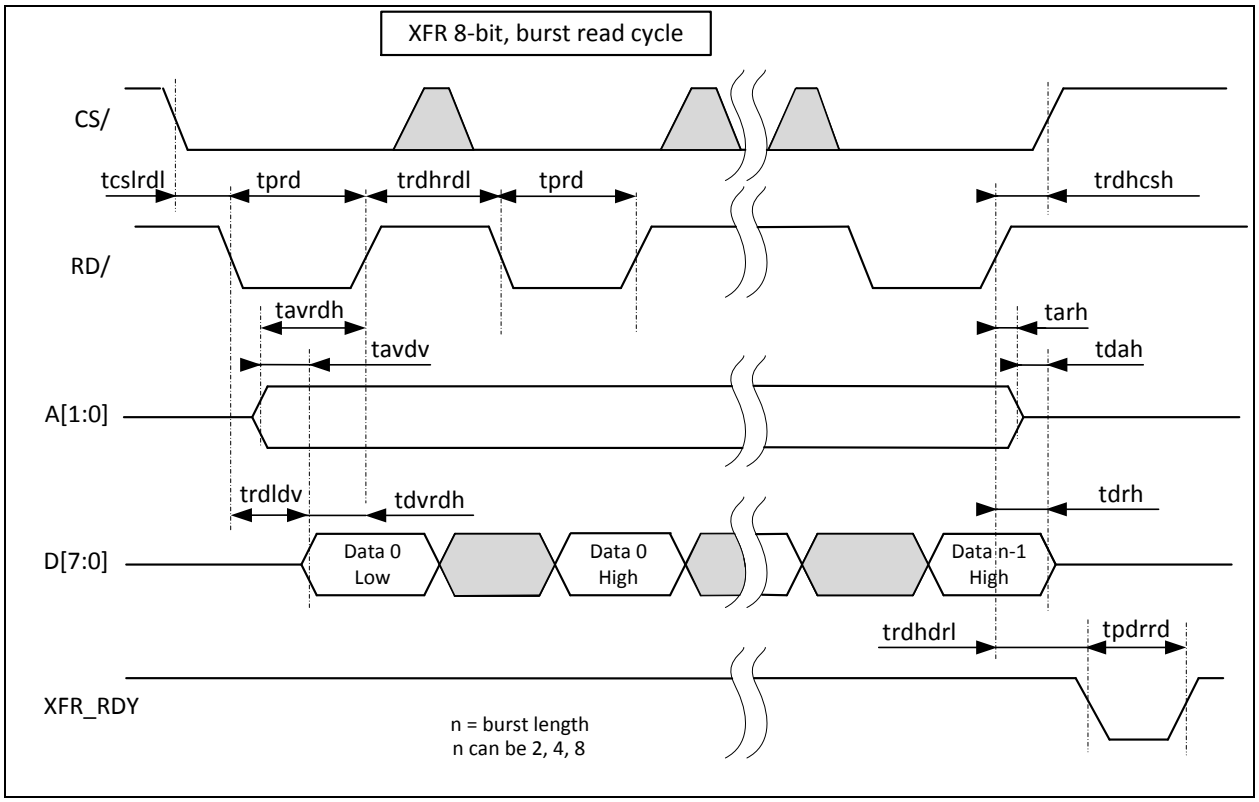

Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to RD/ low	tcslrdl	2 (see note 1)	-	-	ns
RD/ pulse width	tprd	10	-	-	ns
RD/ high to RD/ low	trdhrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	3 (see note 1)	-	-	ns
Address valid to RD/ high	tavrdh	3	-	-	ns
Address valid to data valid	tavdv	-	-	10	ns
RD/ low to data valid	trdldv	-	-	10	ns
Data valid to RD/ high	tdvrdh	3	-	-	ns
Address out hold from RD/	tarh	3	-	-	ns
Data out hold from RD/	tdrh	0	-	10	ns
Data out hold from address out	tdah	0	-	10	ns
RD/ high to XFR_RDY low	trdhdrl	-	-	10	ns
XFR_RDY pulse width in read mode	tpdrrd	15	-	-	ns

Notes:

2. tcslrdl Min and trdhcsh Min can be reduced to 0 ns if 3 ns are added to tprd Min, tarh Min, tdrh Min, tavrdh Min, tdvrdh Min
3. See also §8.8.2.3 Typical timing examples

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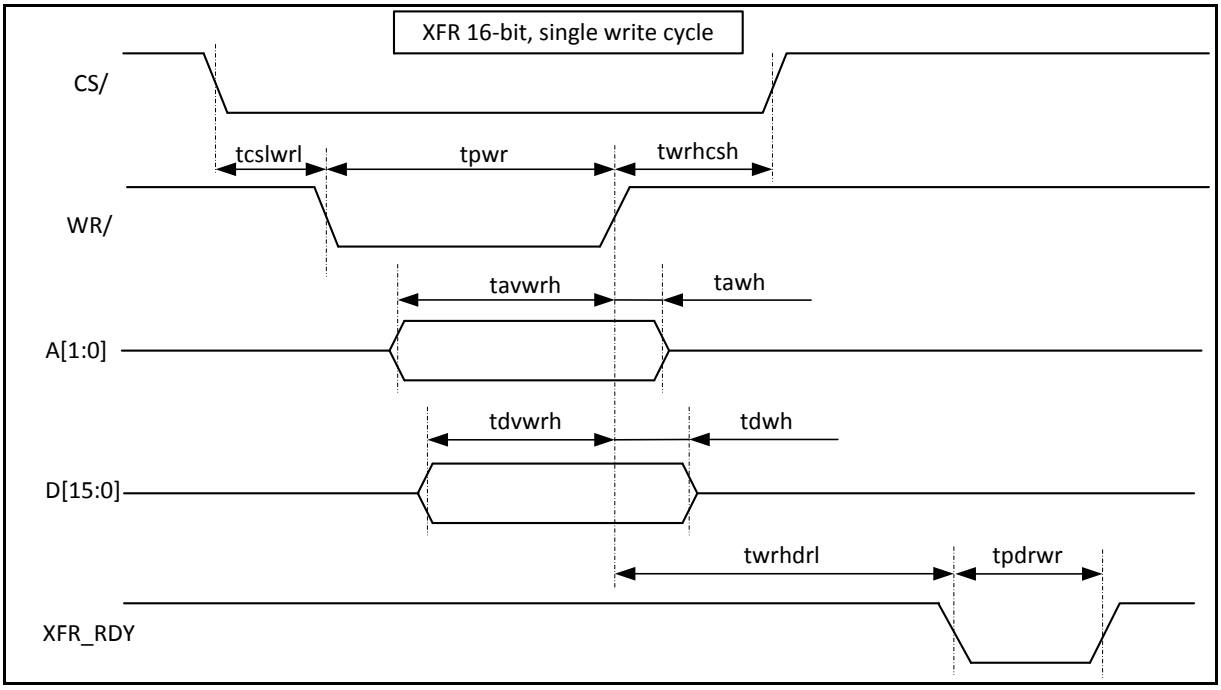
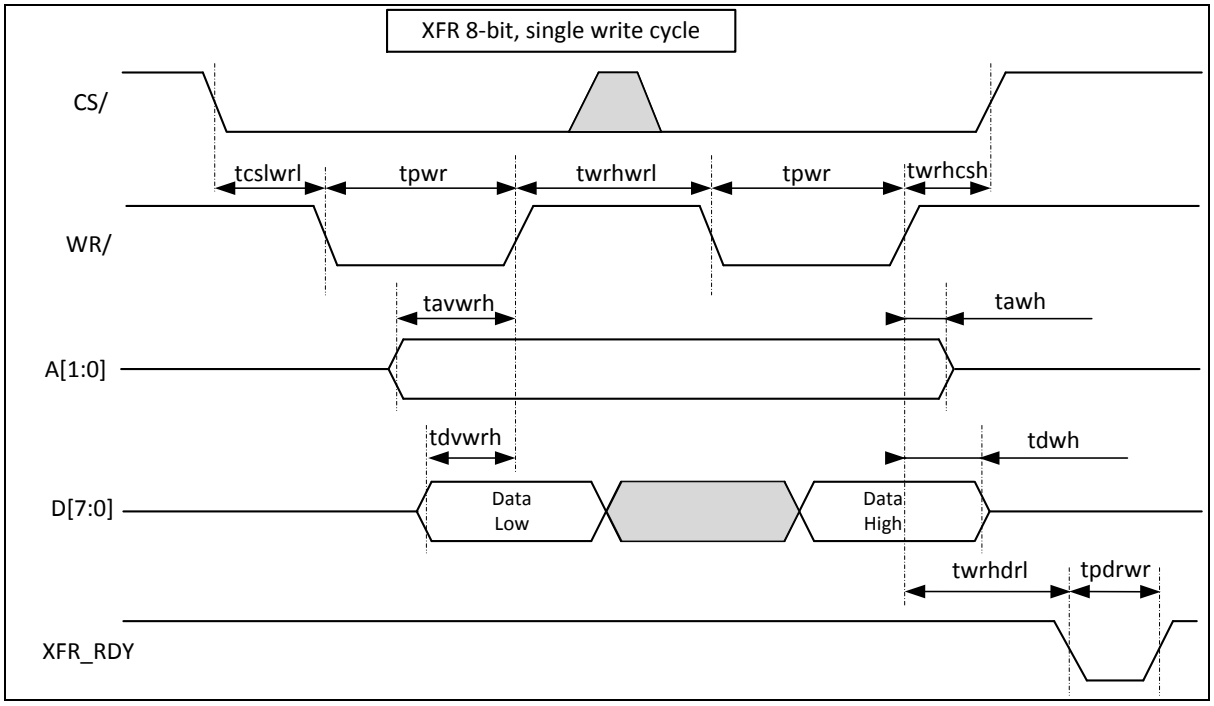
8.8.2.2. HPI mode 1, Write Timing





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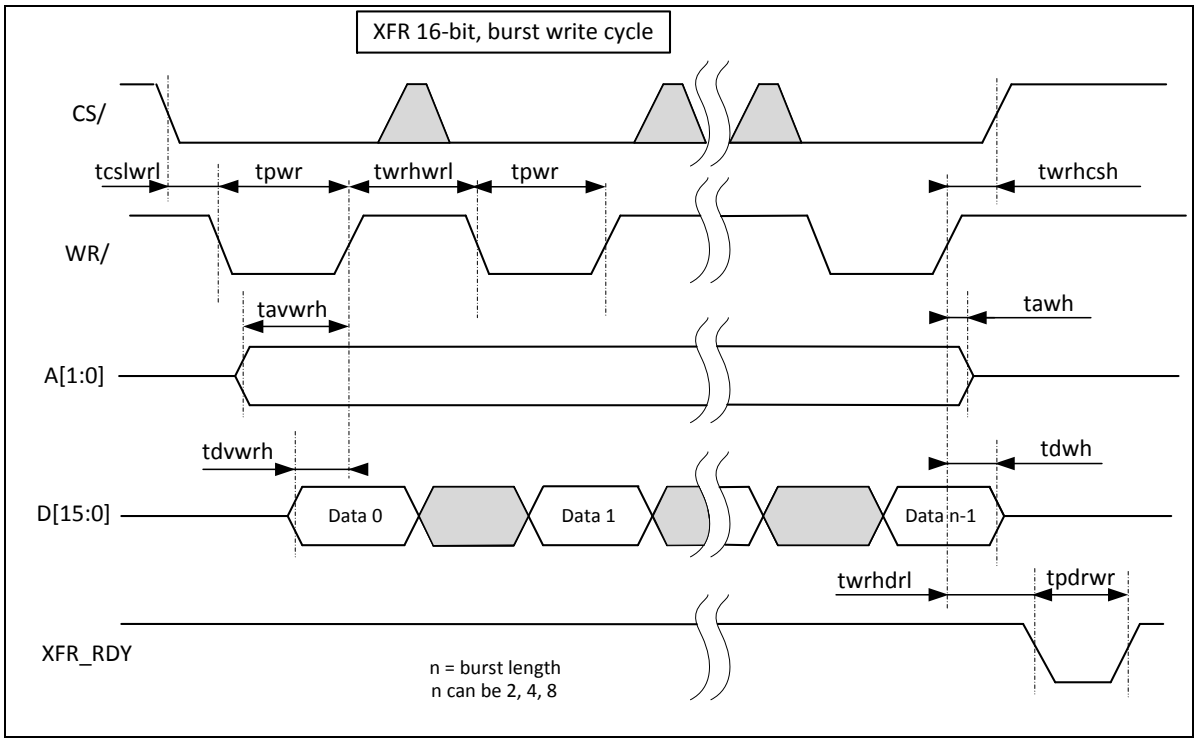

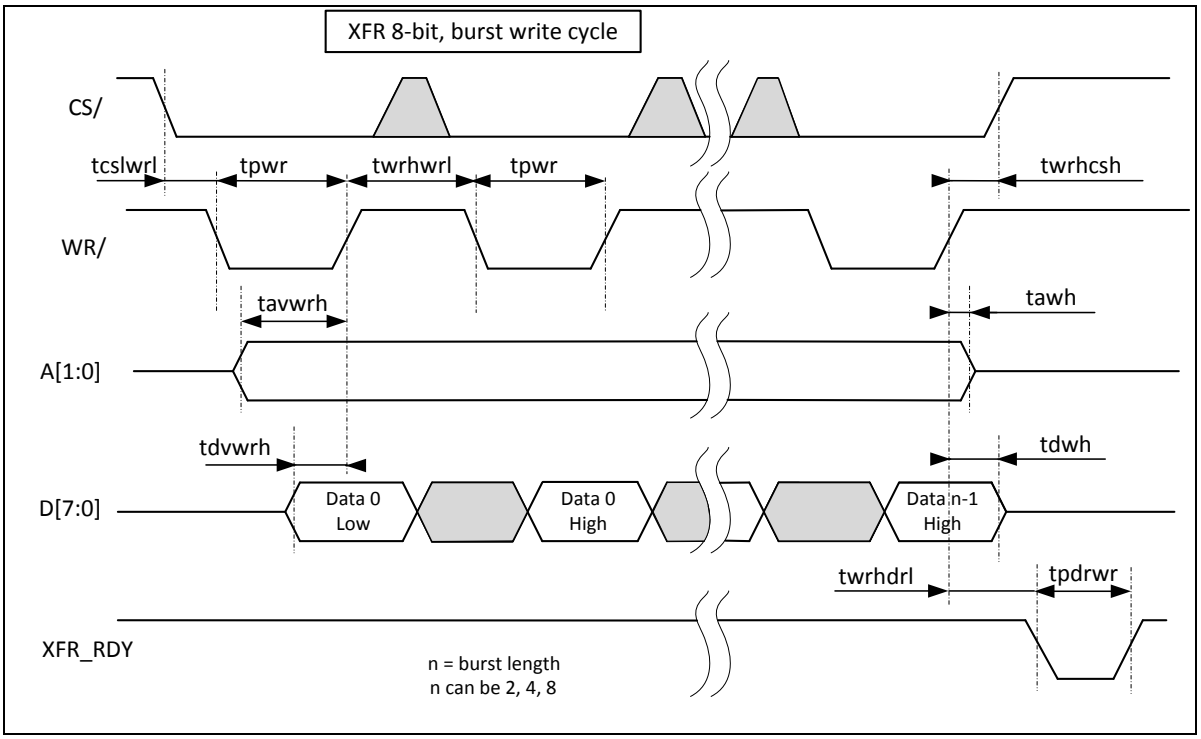

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Parameter	Symbol	Min	Typ	Max	Unit
Chip select low to WR/ low	tcslwrl	2 (see note 1)	-	-	ns
WR/ pulse width	tpwr	5	-	-	ns
WR/ high to WR/ low	twrhwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	3 (see note 1)	-	-	ns
Address valid to WR/ high	tavwrh	3	-	-	ns
Data valid to WR/ high	tdvwrh	3	-	-	ns
Address out hold from WR/	tawh	3	-	-	ns
Data out hold from WR/	tdwh	3	-	-	ns
WR/ high to XFR_RDY low	twrhdrl	-	-	10	ns
XFR_RDY pulse width in write mode	tpdrwr	15	-	-	ns

Notes:

2. tcslwrl Min and twrhcsh Min can be reduced to 0 ns if 3 ns are added to tpwr Min, tawh Min, tdwh Min, tavwrh Min, tdvwrh Min

8.8.2.3. Typical timing examples for sound bank loading via HPI mode 1

1) SDRAM, burst x8, 8-bit mode, no traffic (all P24 stopped)
XFR_READY low typ = 15 to 45 ns
Time for transferring 1Kx16: Write mode=25us, Read mode=32us
---> write a 256Mx16 sound bank = less than 7 seconds

2) SDRAM, burst x8, 16-bit mode, high traffic (all P24 on, 256 voice poly accessing also SDRAM simultaneously)
XFR_READY low typ = 250ns to 400ns (write mode), 150ns to 250ns (read mode)
Time for transferring 1Kx16: Write mode=47us, Read mode=37us
---> write full 256Mx16 sound bank = less than 14 seconds

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8.9. Serial Slave Asynchronous Interface (UART / MIDI)

The SAM5704B can be controlled by an external host processor through this bidirectional serial interface. Firmware can be downloaded at power-up through this interface.

Pins used:
MIDI_IN1, MIDI_OUT1: UART / MIDI port 1
MIDI_IN2, MIDI_OUT2: UART / MIDI port 2

The serial signals on MIDI_IN and MIDI_OUT pins are asynchronous signals following the UART / MIDI transmission standard:

baud rate: programmable up to >400kb/s, typically 31.25 kb/s (MIDI) or 38.4kb/s (COM)
Format: start bit (0), 8 data bits, stop bit (1)

8.10. Serial Slave Synchronous Interface

The SAM5704B can be controlled by an external host processor through this unidirectional serial interface. Firmware can be downloaded at power-up through this interface.

Pins used:
SSCLK, SSYNC, SSDIN (input)
SSINT/ (output)

Data is shifted MSB first. SAM5704B samples an incoming SSDIN bit on the rising edge of SSCLK, therefore the host should change SSDIN on the negative SCLK edge.

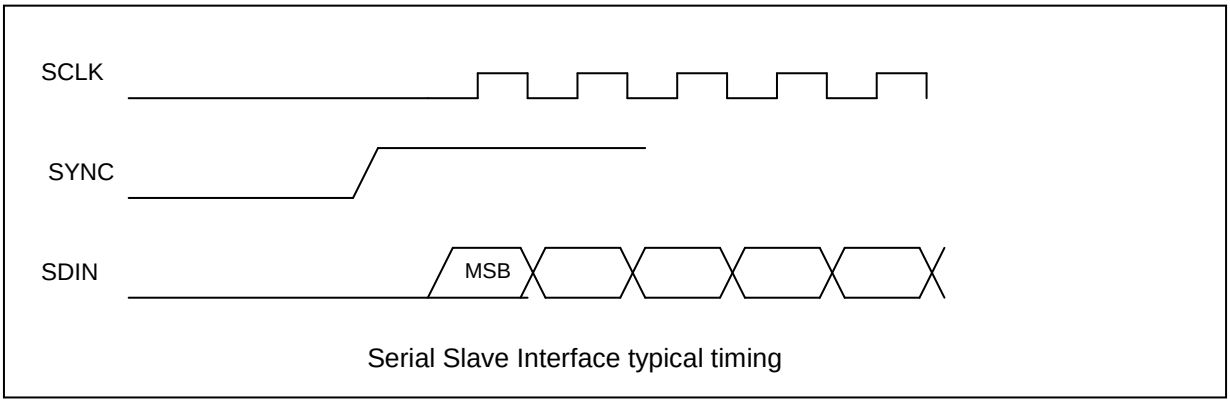
SSYNC allows initial synchronization. The rising edge of SSYNC, which should occur with SSCLK low, indicates that SSDIN will hold MSB data on the next rising SSCLK.

The data is stored internally into a FIFO. Size of FIFO is firmware dependent. Minimum size is 128 bytes. Host should stop sending data as soon as SSINT/ goes high.

When the FIFO count is below 64, the SSINT/ output goes low. This allows the host processor to send data in burst mode.

The maximum SSCLK frequency is fsck/4 (fsck being the system clock frequency. fsck =1/spck).
The minimum time between two bytes is 256 spck.

The contents of the SSDIN data are defined by the firmware.



Serial Slave Interface typical timing

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8.11. I²S Digital audio

Pins used:
CLBD, WSBD (outputs): Audio clocks
DABD7-0: Digital audio outputs (8 * 2 channels)
DAAD7-0: Digital audio inputs(8 * 2 channels)

And optionally
XCLBD0-XWSBD0, XCLBD0-XWSBD0 (inputs): 2 pairs of external clocks for slave mode on DAAD7-0 inputs.

The SAM5704B allows for 16 digital audio output channels and 16 digital audio input channels. All audio channels are normally synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator. However, as a firmware option, the DAAD7-0 inputs can be individually synchronized with incoming XCLBD and XWSBD signals. In this case, the incoming sampling frequencies must be lower or equal to the chip sampling frequency.

The digital audio timing follows the I2S or MSB left standard, with up to 24 bits per sample

The choice of clock factors is done by the firmware. As an example, table below show some possible clock combinations with 12.288MHz Xtal.

Sampling Rate @ Xtal=12.288MHz	CKOUT freq	CKOUT/WSBD freq ratio	CLBD freq	CLBD/WSBD freq ratio
48kHz	12.288MHz	256	3.072MHz	64
48kHz	24.576MHz	512	3.072MHz	64
96kHz	12.288MHz	128	6.144MHz	64
96kHz	24.576MHz	256	6.144MHz	64
192kHz	24.576MHz	128	12.288MHz	64

Note: WSBD/CLBD ratio is always 64.

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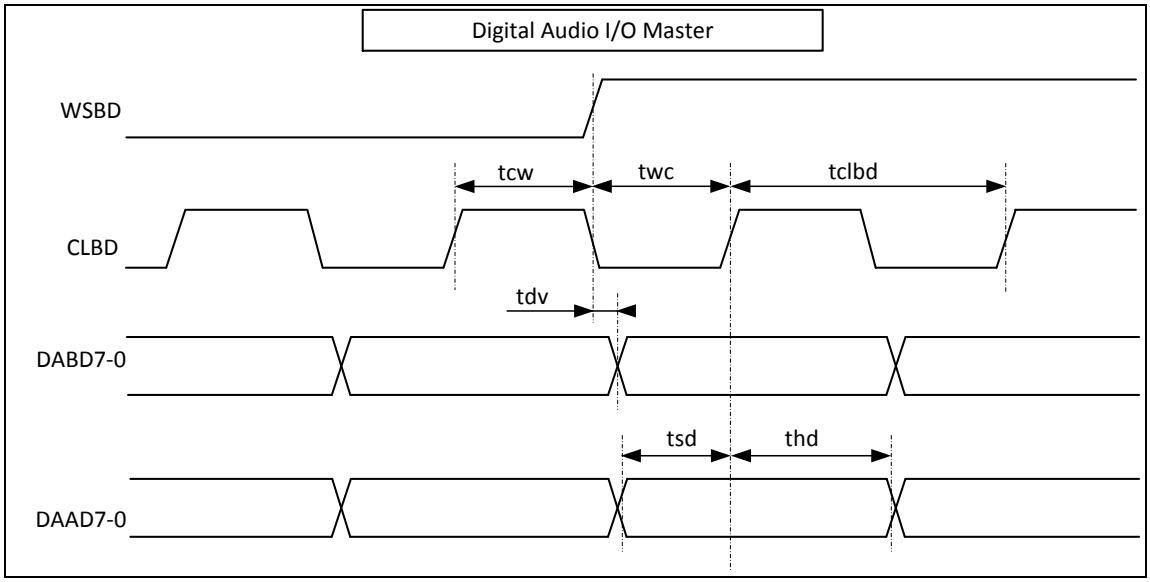
8.11.1. Timing

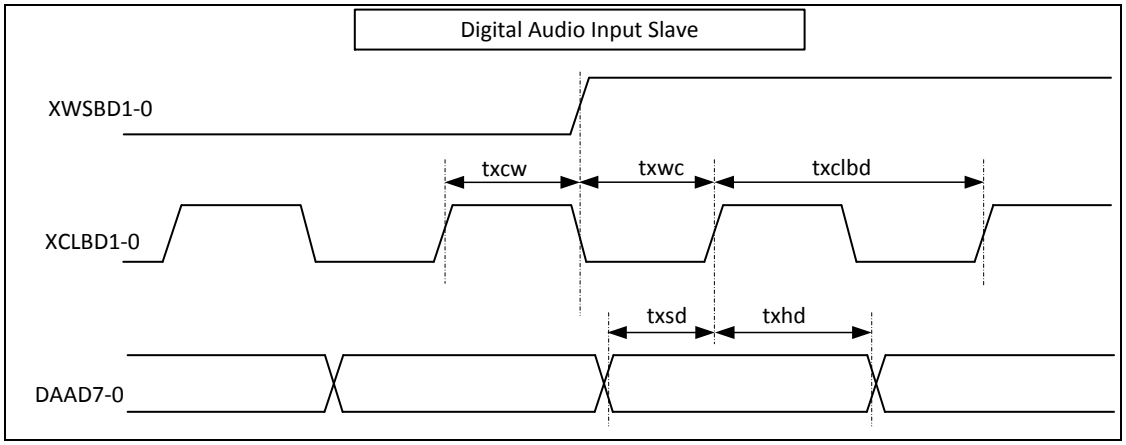
8.11.1.1. Master Mode



cpck is related to CLBD frequency: cpck = 1/(2*CLBD_freq)

Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	cpck -11	-	-	ns
WSBD change to CLBD rising	twc	cpck -11	-	-	ns
DABD valid after CLBD falling	tdv	-11	-	11	ns
DAAD valid prior CLBD rising	tsd	20	-	-	ns
DAAD valid after CLBD rising	thd	20	-	-	ns
CLBD cycle time	tclbd	-	2* cpck	-	ns

8.11.1.2. Slave Mode



xpck is related to XCLBD frequency: xpck = 1/(2*XCLBD_freq)

Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	txcw	20	-	-	ns
WSBD change to CLBD rising	txwc	20	-	-	ns
DAAD valid prior CLBD rising	txsd	20	-	-	ns
DAAD valid after CLBD rising	txhd	20	-	-	ns
CLBD cycle time	txclbd	-	2* xcpck	-	ns

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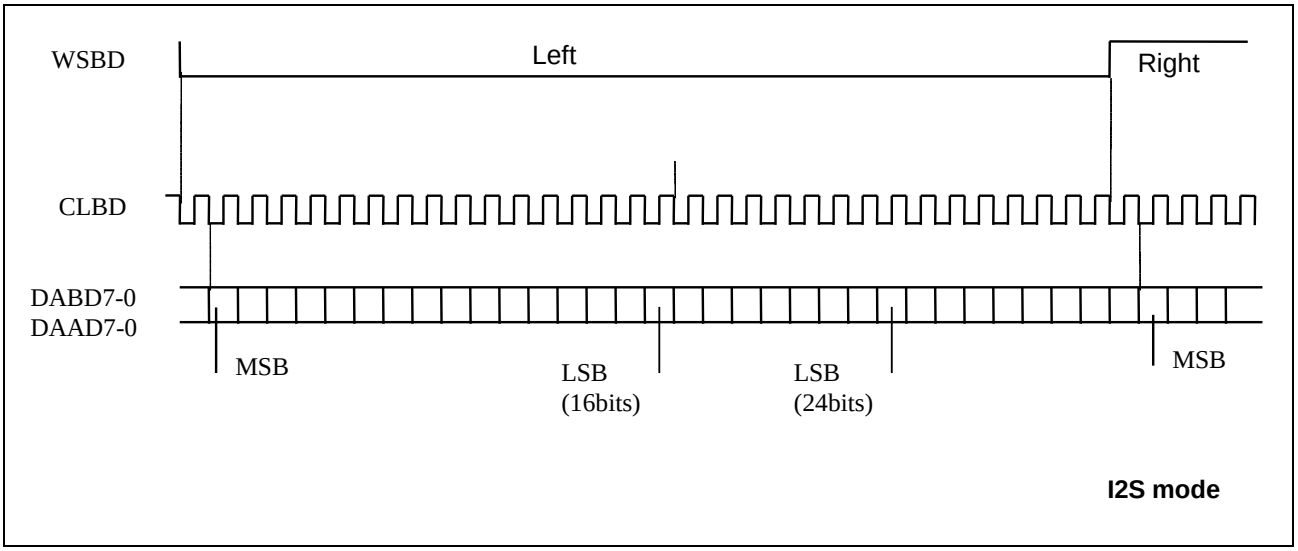
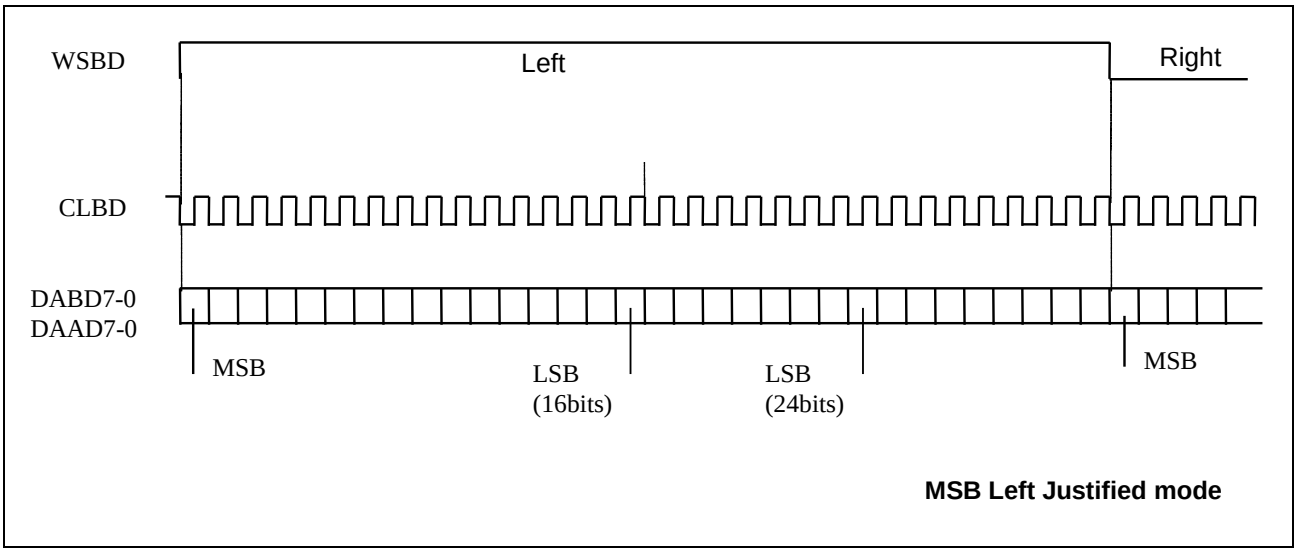
8.11.2. Digital Audio Format

SAM5704B can generate I2S or MSB Left justified digital audio format. Master Clock CLBD can be 128xFs, 256xFs, 512xFs, 192xFs, 384xFS or 768xFs. Format and clock ratio are selected by firmware.



I2S mode



MSB Left Justified mode

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8.12. SPDIF Digital audio

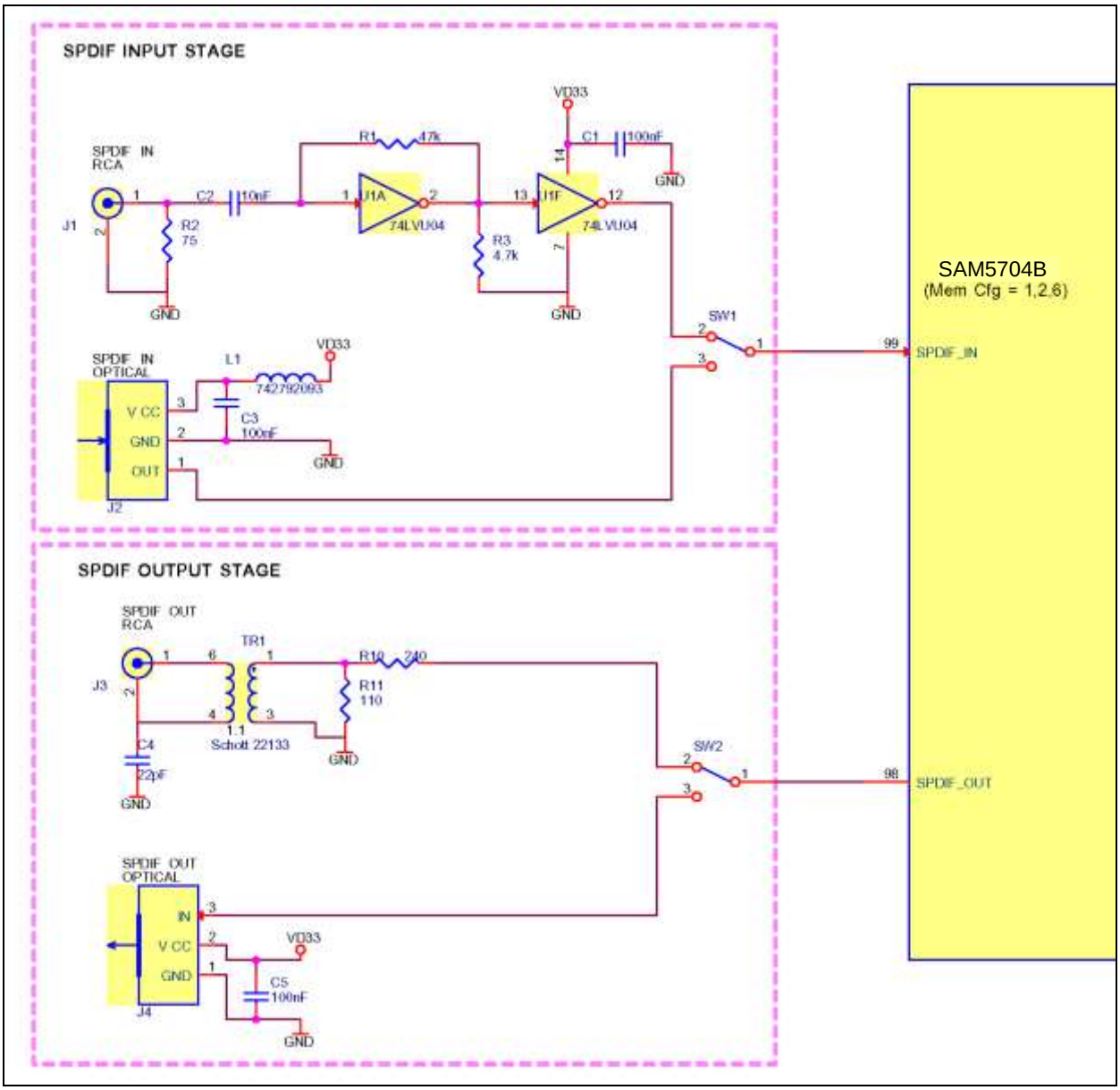
The SPDIF Digital Audio Interface Controller implements the IEC60958 interface features (commonly known as Sony/Philips Digital Interface), a unidirectional and self-clocking interface for connecting digital audio equipment using the linear PCM coded audio samples.
Receiver and Transmitter modes are supported at the same time.

Pins used:
SPDIF_IN: Serial data input
SPDIF_OUT: Serial data output

Data mode capabilities:
- Sample rate from 3kHz to 192kHz
- 24 bit per sample

8.12.1. Reference Schematic

Schematic below is example design for SPDIF IN and OUT interface with SAM5704B.



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8.13. USB 2.0 Ports

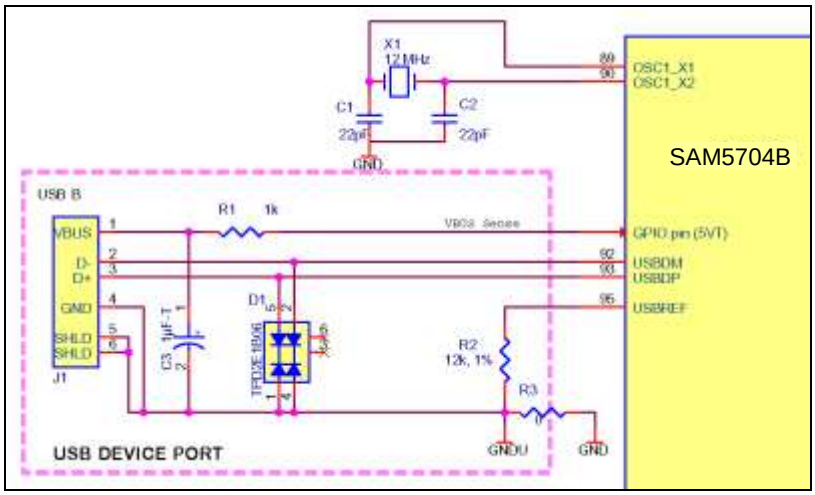
SAM5704B offer one USB 2.0 (High-Speed) port:
It can be can be used as Device, Host or Dual Role.

Pins used:

OSC1_X1-OSC1_X2:	12MHz Crystal connection
USBDM-USBDP:	Differential analog IO
USBREF:	Connection to 12kΩ ± 1% reference resistor
USBID:	A or B device detection in Dual Role Mode (input)

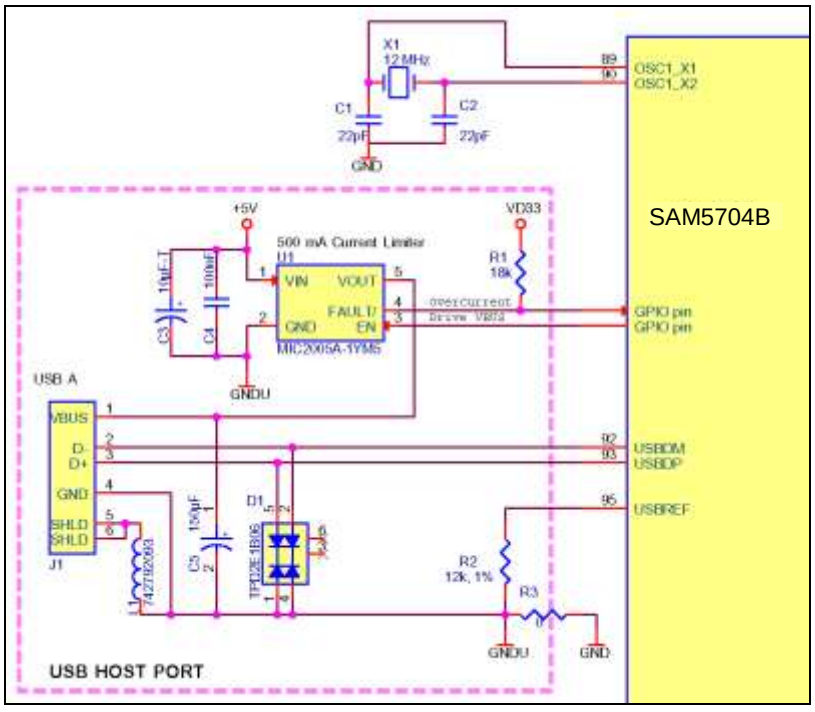
8.13.1. USB Device Port

Schematic below can be used as reference for application with USB Device Port



8.13.2. USB Host Port

Schematic below can be used as reference for application with USB Host Port



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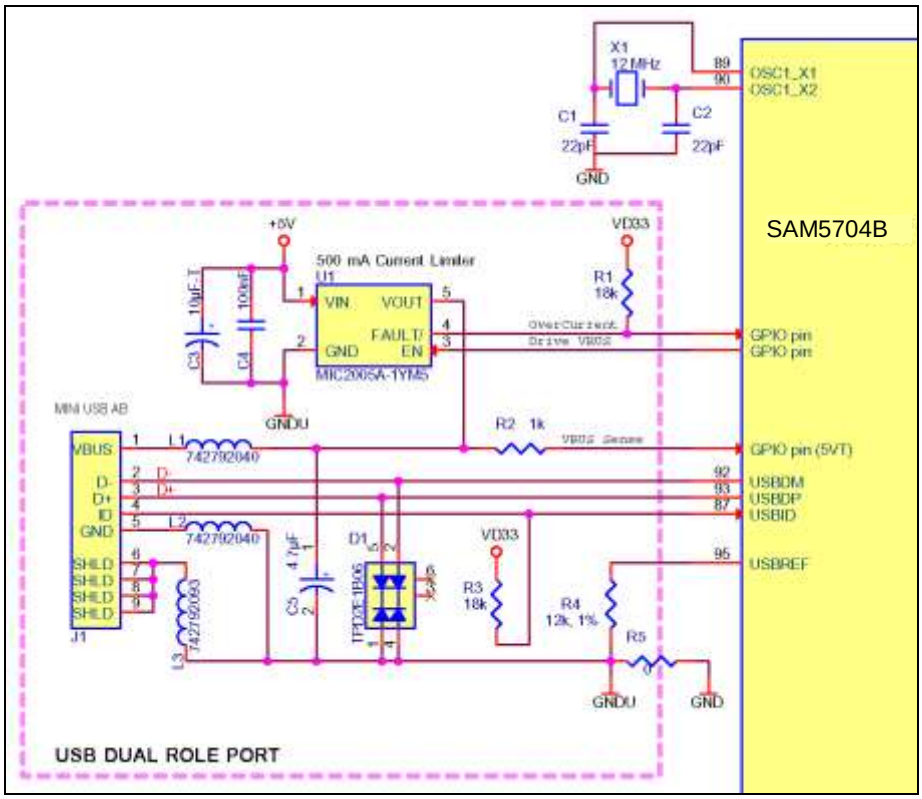
8.13.3. USB Dual Role Port

Schematic below can be used as reference for application with on Dual Role Port.



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8.14. Ethernet Media Access Control

8.14.1. Overview

SAM5704B can access Ethernet through its embedded MAC (Media Access Control) connected to an external Ethernet PHY (Physical transceiver).

Network interface features:
- Support 10/100 data transfer rate
- Reduced Media Independent Interface (RMII)
- MII Management unit for access to the internal PHY registers
- Internal loopback mode

Data link layer functionality:
- Meet the IEEE 802.3 CSMA/CD standard
- Full or half duplex 10/100 (operation)
- Flexible address filtering (Up to 16MAC addresses, 512-bit hash table)
- Flow Control (with automatic Pause and Un-Pause frame generation)
- Statistical Counter for station management (MIB)

Integrated DMA
- Scatter-gather (descriptor based) architecture
- Descriptor “ring” or “chain” structures
- Arbitrary data alignment for the transmit buffers

Transmit/receive dual port RAM interfaces
- Operates as internal configurable FIFOs
- Programmable transmit threshold levels
- Transmit FIFO “store and forward” functionality

Pin used:

REF_CLK:	25MHz RMII reference clock output
ETH_RES/:	Reset output
RX_ER:	RMII Receive Error input
RXD0:	RMII Receive Data 0 input
RXD1:	RMII Receive Data 1 input
CRS_DV:	RMII Carrier Sense/Receive Data Valid input
TXD0:	RMII Transmit Data 0 output
TXD1:	RMII Transmit Data 1 output
TX_EN:	RMII Transmit Enable output
MDC	MII Clock output
MDIO	MII Data I/O

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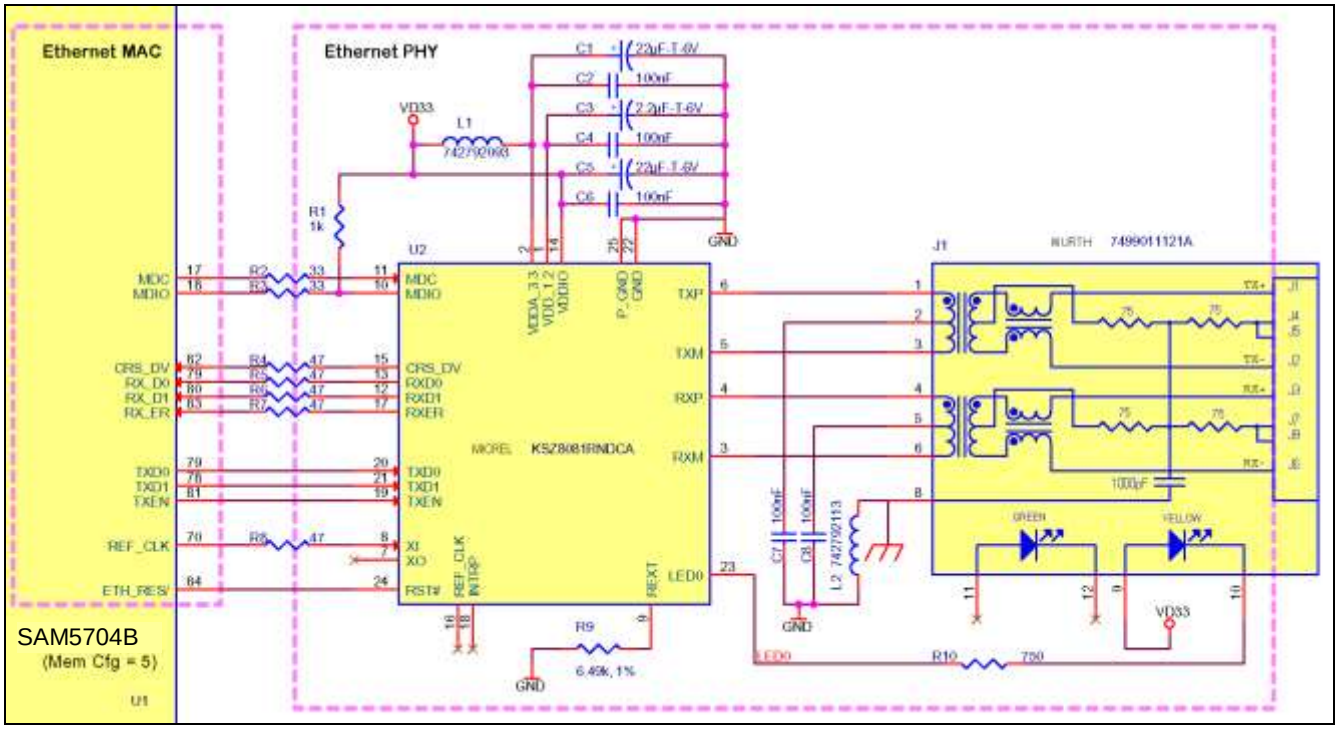
8.14.2. Reference Schematic

Schematic below is example design for Ethernet interface with SAM5704B.
Ethernet PHY is made of Micrel KSZ8081 PHY device + Wurth 7499011121A LAN transformer/connector.



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9. Audio Synchronization

9.1. Synchronization on external audio devices

In professional applications, it can be decided to synchronize SAM5704B audio processing on external audio flow(s) from USB, SPDIF or Ethernet interfaces. Another professional feature is synchronization on external word clock.

9.1.1. Principle

- Audio clock frequency is extracted from incoming audio flow or from external word clock and is compared with frequency currently used for internal audio processing.
- Comparison result is used to control the internal PWM generator.
- PWM generator output is filtered, and then, can drive an external VCXO.
- VCXO clock output is used as master clock for internal audio processing.

As a result, clock frequency for internal audio processing is perfectly enslaved to incoming audio flow.

Pin used:

OSC1_X1, OSC1_X2:	Connection to 12MHz crystal for USB, Ethernet and system boot.
X1:	Clock input for audio system clock from VCXO
PWM:	PWM output
XWSBD0 (optional):	Input for external Word Clock

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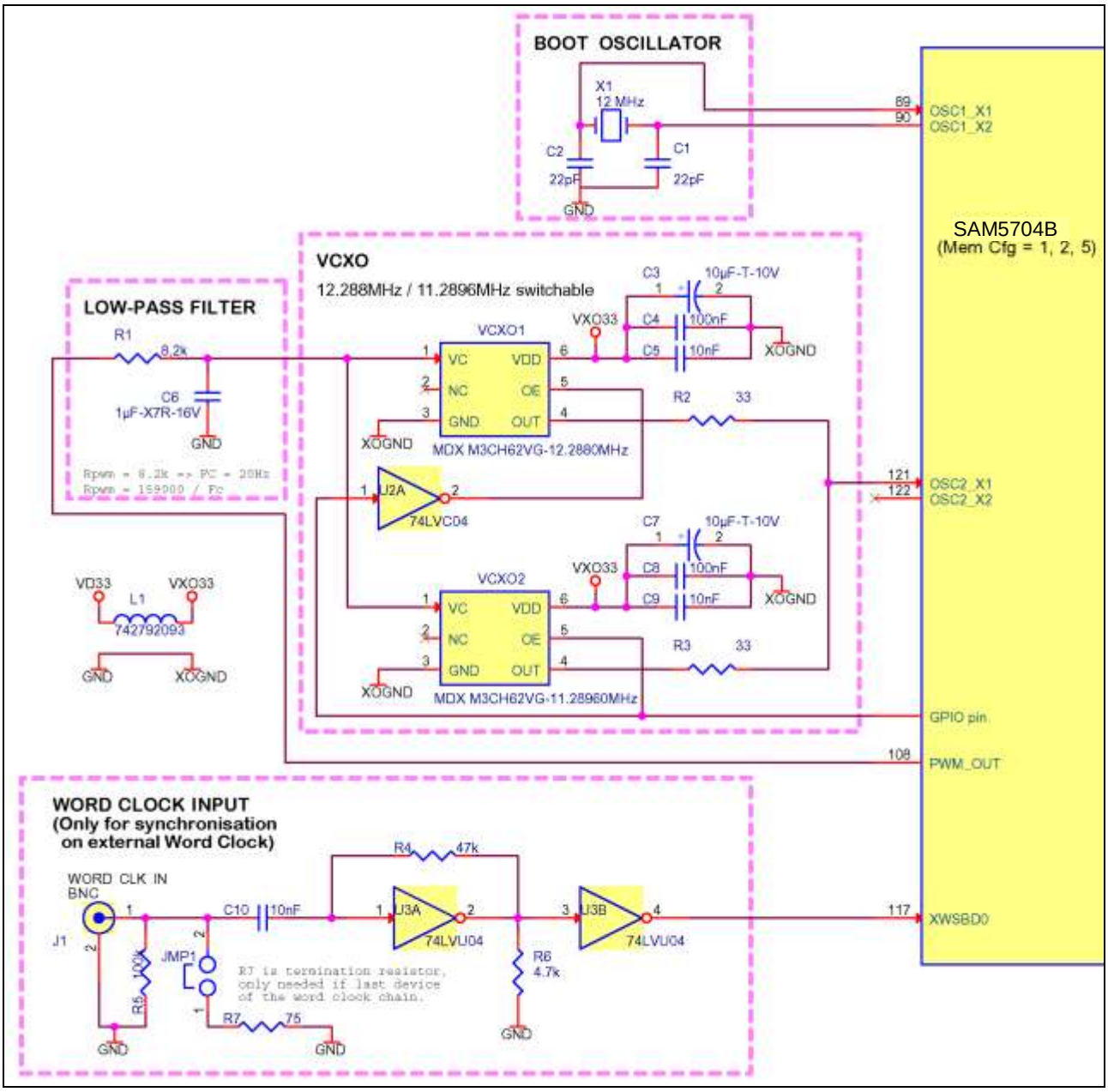
9.1.2. Reference schematic

Schematic below can be used as reference for synchronization on external audio flowing and optionally on external word clock.



- At start-up system runs on USB/Ethernet oscillator used as Boot oscillator.
- When environment is stabilized, firmware switches system and audio clock source from boot oscillator to second oscillator input OSC2_X1 driven by VCXO clock.

Notes:
- PCB design around VCXO is sensitive. See VCXO manufacturer relative application notes

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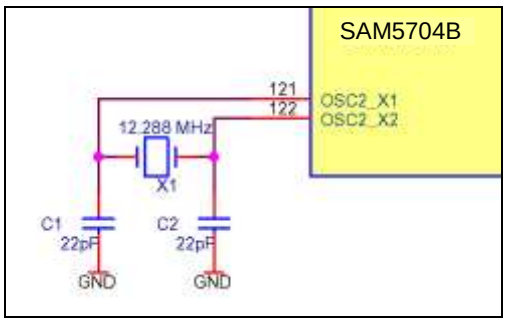
10. Recommended Crystal Compensation

10.1. OSC2_X1 – OSC2_X2



C1 and C2 should be chosen in range 12pF-27pF. Different values lead to different oscillation characteristic and can be selected based on board layout considerations.
External feedback resistor should be avoided because there is an internal feedback resistor.

10.2. OSC1_X1 – OSC1_X2

Crystal connection on OSC1_X1-OSC1_X2 follows the same off-chip components recommendation than crystal connection on OSC2_X1-OSC2_X2

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11. Reset and Power Down

During power-up, the RST/ input should be held low until the core is stabilized in reset state, which takes 10ms Max.
After the low to high transition of RST/, following happens:

- Oscillator OSC1 is started
- P16 program execution starts in built-in ROM
- PLL is started and stabilized after 2.8 ms typ
- P16 application program loading starts.

If RST/ is asserted low then the crystal oscillators and PLLs will be stopped.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256
- ADC can be disabled
- Controllers for USB, Ethernet or SDRAM can be individually switched off

11.1. Power-up sequence

At power-up the following sequence is executed:

1. STIN is sensed. If HIGH, then the built-in debugger is started.
2. If MC2-0 bits were preprogrammed they are read from eFuse. Otherwise MC2-0 pins are sensed and corresponding Memory Config is set
3. ROM boot tries to identify source for firmware. For that it tries to find “DR” marker for Dream firmware. This step is done in slow mode (PLL not started). During this step, rom boot set the minimum of primary functions to avoid any potential conflict of some pins. Accesses to memories are done with longest access time, most simple protocol (accessing for example Quad SPI memory in single mode rather than quad mode). ROM boot searches source in following order:
   a) Main Memory. According to Memory Config, Main Memory can be: NOR Flash, NAND Flash or Quad-SPI NOR Flash.
   b) Serial Flash/EEPROM on Multi-Purpose (Q)SPI Port
4. If valid firmware has not been found, firmware download from a host processor is assumed into internal RAM (40k x 16 max) through 8-bit Parallel (if eFuse 14 not blown, default), Serial Slave Synchronous (if eFuse 14 blown) or Serial Slave Asynchronous (UART / MIDI_IN1) port.

<u>If Host CPU is connected on 8-bit Parallel Interface (eFuse 14 not blown, default):</u>

a) The byte 0ACh is written to the host. The host checks status and can recognize that the chip is ready to accept program download.
b) The host sends the Boot_Info table (low byte first, 20 * 2 bytes). Boot_Info table contains info on firmware size, primary and secondary functions setting, memory and software config. The Boot_Info table is generated by SamVS , and is located in the firmware binary file at word addresses 1-20.
c) SAM5704B sends ACh when initializations are ready
d) The host sends the SAM5704B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
   a. "DownLoadSize" is defined in the Boot_Info table at word address 3.
e) The byte 0ACh is written to the host. The host checks status and can recognize that the chip has accepted the firmware.
f) SAM5704B starts the firmware.

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Note: Be aware that at boot time the IRQ signal is not used, the Host CPU must read the port status register (TE/RF bits) before sending or reading a data byte to/from SAM5704B via 8-bit parallel port.

If Host CPU is connected on Serial Slave Synchronous Interface (eFuse 14 must be blown):

a) The host sends the Boot_Info table (low byte first, 20 * 2 bytes, see description above).
b) The host sends the SAM5704B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
c) SAM5704B starts the firmware.

Note:
For debug purpose of the download through Serial Slave Synchrounous interface, if eFuse 15 is blown, the acknowledge bytes ACh can be checked on the MIDI_OUT1 pin.

If Host CPU is connected on Serial Slave Asynchronous Interface / UART (MIDI_IN1):
Download through MIDI_IN1 (UART) is always available (there is no eFuse to be blown). However, the acknowledge bytes ACh are sent on MIDI_OUT1 only if eFuse 15 is blown.

a) If eFuse 15 is blown, the byte 0ACh is sent on MIDI_OUT1 to the host.
Note: this first ACh byte may be difficult to be recognized by host because during power-up the MIDI_OUT1 pin is in undefined state and host may receive many invalid midi data before receiving this ACh byte. This first ACh byte is more intended for debug purpose or scope checking.
b) Host sends at 38.4Kbit/s the 2 bytes 52h and 44h on MIDI_IN1
Note: SAM5704B automatically disables the download through MIDI_IN1 if the 2 first bytes received are not 52h and 44h.
c) Then host sends at 38.4Kbits/s the Boot_Info table (low byte first, 20 * 2 bytes, see description abaove). A new baud rate is defined in the Boot_Info table at word address 4.
d) If eFuse 15 is blown, SAM5704B sends ACh on MIDI_OUT1 (at new baud rate).
e) The host sends at new baud rate the SAM5704B firmware binary from word address 400h, 2*DownLoadSize bytes, low byte first.
f) If eFuse 15 is blown, the byte 0ACh is sent to the host (new baud rate).
g) SAM5704B starts the firmware.

Note: When using download through MIDI_IN1, the 2 other host interfaces must not be active during download:
- if eFuse 14 not blown (Host 8-bit Parallel Interface): pin CS/ (or pin WR/) of 8-bit parallel interface must be high.
- if eFuse 14 blown (Serial Slave Synchronous Interface): clock pin SSCLK of Serial Slave Synchronous interface must be idle

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11.2. Pin status in Power-down mode

Table below shows the status of each I/O pin in Power-down mode (RST/ Low)

Pin name	Status in Power-down mode
VIN	ANA IN
RST/	IN driven Low
TEST	IN with Pull-down resistor
STIN	IN with Pull-down resistor
STOUT	IN with Pull-up resistor
CKOUT, CLBD, WSBD	IN with Keeper resistor
MIDI_IN1, MIDI_OUT1	IN with Keeper resistor
All Memory pins (MEM)	TRISTATE output
All other I/O pins	IN with Keeper resistor

Note:

- Keeper resistor can be pull-up or to pull-down resistor. This will depend on logic state at the pin where it is connected when switching to Power-down mode.
    - If logic state is ‘Low’ when entering Power-down mode, keeper resistor will be pull-down
    - If logic state is ‘High’ when entering Power-down mode, keeper resistor will be pull-up

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12. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

12.1. GND, VD33, VC12, VD12 distribution, decoupling

All GND, VD33, VC12, VD12 pins should be connected. A GND plane is strongly recommended. The board GND, VD33, VC12 and VD12 distribution should be in grid form.

Recommended VD12 decoupling is 0.1µF at each VD12 pin of the IC with additional 10µFT on two opposite sides

VC12 pin requires 10µFT +100nF.

Recommended VD33 decoupling is 0.1µF at half of VD33 pins. 10nF should be connected at the other half of VD33 pins. 10µFT should be also added on two opposite sides.
VD33R requires a single 10µFT decoupling.
VD330 requires a single 100nF decoupling.
VD33U requires 10µFT+100nF+10nF capacitors.

12.2. Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

12.3. Busses

Parallel layout from D15-D0 and MA26-MA0/MD15-MD0 should be avoided. The D15-D0 bus is an asynchronous type bus. Even on short distances, it can induce pulses on MA26-MA0/MD15-MD0 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the D16-D0 bus, which connects both to the host and to SAM5704B GND.

A ground plane should be implemented below the MA26-MA0/MD15-MD0 bus, which connects both to the NOR Flash grounds and to SAM5704B.

A ground plane should be implemented below the MA18-MA0/MD15-MD0 bus, which connects both to the SRAM grounds and to SAM5704B.

A ground plane should be implemented below the NDIO8-NDIO0 bus, which connects both to the NAND Flash grounds and to SAM5704B.

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12.4. SDR SDRAM

For SDRAM following layout rules should be applied:

- 4 layer PCB is needed for SDR SDRAM. Layer 1 = Signal + Ground plane, Layer 2 = Ground plane, Layer 3 = Signal + Power Supply Plane, Layer 4 = Signal + Ground plane

- All DRDQ15-DRDQ0, DRDM0-DRDM1 should be routed together and should have same length, considering all the SDRAM devices. It means that each DRDQx signal should have the same length from its SAM5704B DRDQx pin to each of the DRDQx pin of each SDRAM device. It also means that all the DRDQx and DRDMx signals should have the same length. Tolerance should be lower than +/-0.5mm.

- All DRDA13-DRDA0, DRDBA1-DRDBA0 should be routed together and should have the same length, considering one SDRAM device. It means that all the DRDAx/DRDBAx signals should have a same length L1 from SAM5704B to the first SDRAM device and a same length L2 from SAM5704B to the second SDRAM device,.... Tolerance should be lower than +/-2mm.

- DRRAS/, DRCAS/, DRWE/, DRCKE should be routed together and should have the same length.

- SDRAM systems have only a single-ended clock (DRCK), so the important trace-matching relationship is not to a second differential clock trace but instead to the other groups. Match clock traces to data group traces within ±12mm. If multiple clocks are transmitted from the controller to components, all clock traces should be equivalent to within ±0.5mm. Matching trace lengths to this level of accuracy helps minimize skew.
  It is also needed to match clock traces to each signal trace in the address and command groups to within ±10mm. If clock traces cannot be matched to the trace lengths of these groups within 10mm, then all clock trace lengths must be increased as a group. The longest-to-shortest trace-length difference must be ≤20mm, so both longest and shortest traces determine how much length must be added to all clock lines.

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12.5. ESD and EMI

Below are some tips that allow reaching good protective level again EMI and ESD with SAM5704B. This list is no exhaustive.

- Equipotentiality of the ground plane is a major point to avoid weakness against EMI. The 4 layer design is the best solution. When 2 layer design, the unused zones of the component side should be filled with ground planes connected with a lot of through holes to the ground plane of the solder side.

- High speed clock and signals trace should be short and shielded. Serial resistor or RC filter can be added close to the source to filter harmonics.

- Main power supply, before regulators should be protected with T filter like Murata NFM41PC204F1H3 and serial choke coil like LQH43CN220K03

- Connectors should be protected. EMI filters like Murata NFM21CC102R1H3 should be implemented on the clock and data lines, close to their connection on the connectors. Power supply lines can be protected with Murata BLM21RK102SN1 or Wurth 742792093.

- Each power supply pin of SAM5704B and of all active components should be decoupled with 100nF X7R capacitor and 470pF NPO or COG capacitor. A 10µF capacitor should be added close to the SAM5704B Xtal.

- Each active component should be isolated from the main power supply with a serial inductor on its power supply lines. Murata BLM21RK102SN1 or Wurth 742792093 can be used for this.

- Address, Data, Chip select, Reset signals for SAM5704B should be isolated from their environment with serial 33 Ohm resistor close to SAM5704B.

- Data, clock lines signals for DAC should be isolated from their environment with serial 22 Ohm resistors close to the DAC.

- On sensitive lines like Reset, 470pF NPO or COG capacitor can be added, close to SAM5704B.

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13. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (WinXP and up). Within the environment, it is possible to:

- Edit
- Assemble / Compile (C Compiler for P16XT included) and build firmware binary file
- Debug on real target (In Circuit Emulation)
- Program external NOR Flash, NAND Flash, or Serial Flash/EEPROM on target.

Separated tools allowing programming the internal eFuses of SAM5704B, e.g. “ProgSam” provided by Dream for in-circuit programming of eFuses and Firmware/sound bank.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using serial communication at 57.6 kbauds. Dream provides a USB debug interface (5000DBG-IF) for easy use.

A library of frequently used functions is available within the SamVS-C development package (5704xx-C-PDK). Thus time to market is optimized by testing directly on the final prototype.

Dream engineers are available to study customer specific applications.

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